



# P67H2-A3

Rev : 1.0

ECS CONFIDENTIAL

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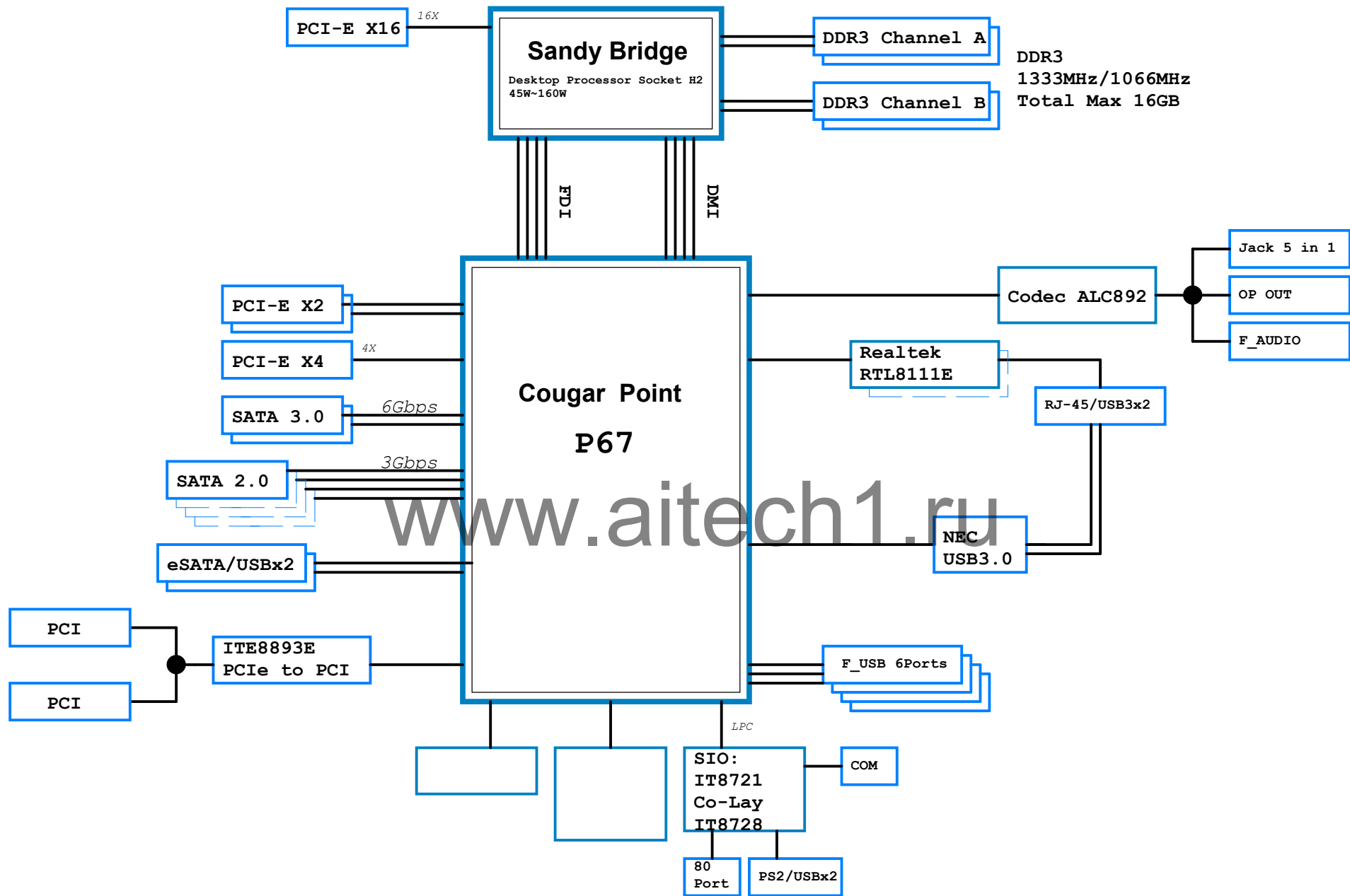
## REVISION HISTORY:

Rev	Date	Notes
V.A	2010/04/16	Initial version
V.B	2010/06/22	
V.1.0	2010/08/09	

## NOTE:

Design by 428971\_428971\_Sugar\_Bay\_and\_BromolowWS\_PDG\_Rev\_0\_8.pdf,  
428880\_428880\_Cougar\_Point\_Desktop\_Ballout\_Mech\_Package\_Rev1p0.zip

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## 3PIO function

Pin Name	Power Well	Usage	Default Status
GPIO0	VCC3	FP_AUD_DETECT	GPI
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GP6_BOMDET3	GPI
GPIO7	VCC3	GP6_BOMDET4	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO11	3VSB	GP6_BOMDET4	Native
GPIO12	3VSB	GP6_BOMDET4	Native
GPIO13	3VSB	GP6_BOMDET4	GPI
GPIO14	3VSB	USB_OC_L7	Native
GPIO16	VCC3	Reserve for TPM	GPI
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO34	VCC3	GPIO34_TCM_PST_L	GPI
GPIO38	VCC3	GPIO38_TCM	GPI
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO68	VCC3	GPIO68_USBDDET1	GPI
GPIO69	VCC3	GPIO69_USBDDET2	GPI
GPIO70	VCC3	GPIO70_USBDDET3	Native
GPIO71	VCC3	Reserve for TPM	Native
GPIO72	3VSB	GPIO72_BOMDET5	Native

## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		SIO_BEEP	
GP23		Power LED	
GP22		Power LED	
GP52		FAN_TAC2	
GP51		FAN_CTL2	
GP37		FAN_TAC3	
GP36		FAN_CTL3	
GP30		8723_ATXPWRGD	
GP26		COM	
GP27		COM	
GP24		COM	
GP25		COM	
GP21		COM	
GP20		COM	
GP17		COM	
GP12		SIO_PCIRST1_L	
GP11		SIO_PCIRST2_L	
GP14		PWRGD1	
GP62		KBRST_L	
GP44		SIO_PWRBTN_L	
GP54		LPC_PME_L	
GP43		FP_PWRBTN_L	
GP42		SIO_PSON_L	
GP17		COM	
GP56		MCLK	
GP57		MDATA	
GP60		KCLK	
GP61		KDATA	
GP10		SIO_PCIRST3_L	
GP55		RSMRST_R_L	

## PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down · No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up · intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up · "topblock swap" mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up · Integrated 1.05V VRM Enable
GNT1# / GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up · The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up · The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TVS	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

Table 7-1. Power On Strapping Options

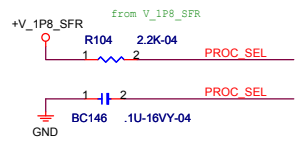
	Symbol	Strapping Event	Value	Description
JP2	Flashseg1_EN	Internal VCC-OK/ LRESET#	1	Disable
Pin 122			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
Pin 126			0	Enable K8 power sequence function
[JP3,JP5]	FAN_CTL_SE L	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
Pin 124 & Pin 46			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.

## Elitegroup Computer Systems

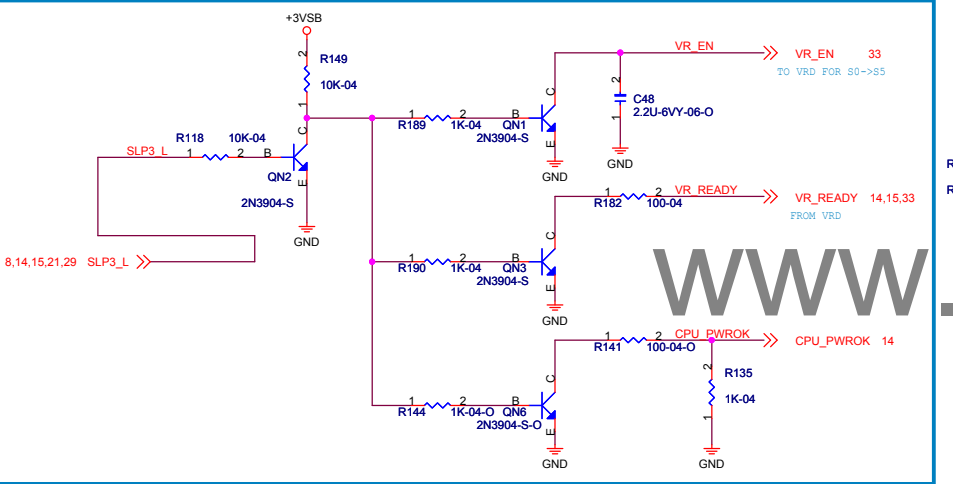
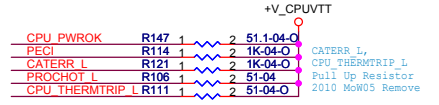
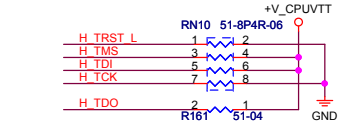
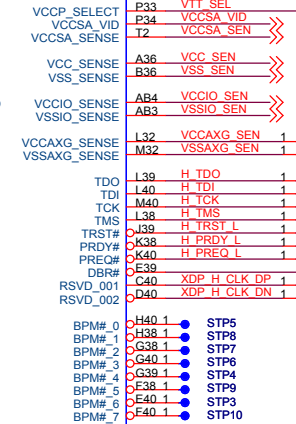
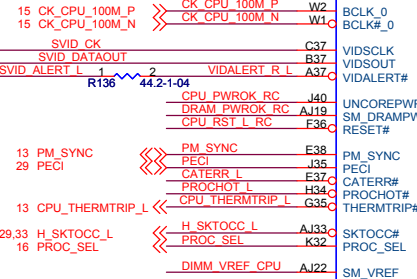
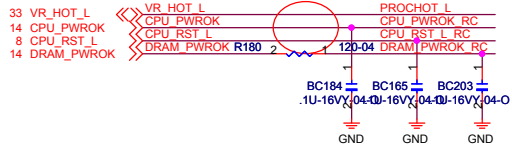
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30-GPIO Function Map			
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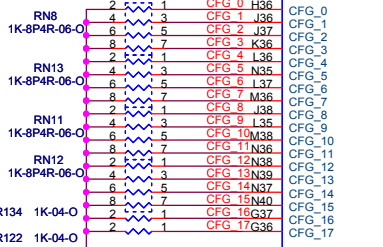




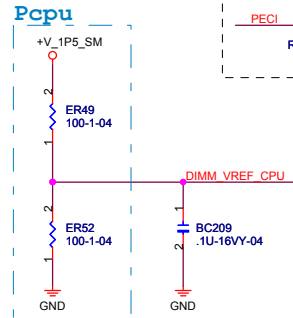
DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



Power Down Sequencing Circuit



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LGA-1155P-S



Place Popu in Socket Cavity.

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0] X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

**Elitegroup Computer Systems**

Title: **CPU - MISC**

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9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M DQS A N[0..7]
9 M_MA_A[0..15]	← M MA A[0..15]
9 M_BS_A[0..2]	← M BS A[0..2]
9 M_CS_A_L[0..3]	← M CS A L[0..3]
9 M_CKE_A[0..3]	← M CKE A[0..3]
9 M_ODT_A[0..3]	← M ODT A[0..3]
9 M_CLK_A_P[0..3]	← M CLK A P[0..3]
9 M_CLK_A_N[0..3]	← M CLK A N[0..3]
9 M_WE_A_L	← M WE A L
9 M_CAS_A_L	← M CAS A L
9 M_RAS_A_L	← M RAS A L

DDR3 CH.A

9,10 DDR3\_DRAMRST\_L ← DDR3\_DRAMRST\_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M DQS B N[0..7]
10 M_MA_B[0..15]	← M MA B[0..15]
10 M_BS_B[0..2]	← M BS B[0..2]
10 M_CS_B_L[0..3]	← M CS B L[0..3]
10 M_CKE_B[0..3]	← M CKE B[0..3]
10 M_ODT_B[0..3]	← M ODT B[0..3]
10 M_CLK_B_P[0..3]	← M CLK B P[0..3]
10 M_CLK_B_N[0..3]	← M CLK B N[0..3]
10 M_WE_B_L	← M WE B L
10 M_CAS_B_L	← M CAS B L
10 M_RAS_B_L	← M RAS B L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AL1	SA_MA_5
M_DATA_A6	AL2	SA_MA_6
M_DATA_A7	AN1	SA_MA_7
M_DATA_A8	AN4	SA_MA_8
M_DATA_A9	AR3	SA_MA_9
M_DATA_A10	AR4	SA_MA_10
M_DATA_A11	AN2	SA_MA_11
M_DATA_A12	AR2	SA_MA_12
M_DATA_A13	AR1	SA_MA_13
M_DATA_A14	AR2	SA_MA_14
M_DATA_A15	AR1	SA_MA_15
M_DATA_A16	AV2	SA_MA_16
M_DATA_A17	AW3	SA_MA_17
M_DATA_A18	AV5	SA_MA_18
M_DATA_A19	AU2	SA_MA_19
M_DATA_A20	AU3	SA_MA_20
M_DATA_A21	AU5	SA_MA_21
M_DATA_A22	AY5	SA_MA_22
M_DATA_A23	AY7	SA_MA_23
M_DATA_A24	AU7	SA_MA_24
M_DATA_A25	AV9	SA_MA_25
M_DATA_A26	AU9	SA_MA_26
M_DATA_A27	AV7	SA_MA_27
M_DATA_A28	AW7	SA_MA_28
M_DATA_A29	AW7	SA_MA_29
M_DATA_A30	AY9	SA_MA_30
M_DATA_A31	AU35	SA_MA_31
M_DATA_A32	AW37	SA_MA_32
M_DATA_A33	AU39	SA_MA_33
M_DATA_A34	AW35	SA_MA_34
M_DATA_A35	AY36	SA_MA_35
M_DATA_A36	AU38	SA_MA_36
M_DATA_A37	AU37	SA_MA_37
M_DATA_A38	AR37	SA_MA_38
M_DATA_A39	AN37	SA_MA_39
M_DATA_A40	AR39	SA_MA_40
M_DATA_A41	AR38	SA_MA_41
M_DATA_A42	AN38	SA_MA_42
M_DATA_A43	AR39	SA_MA_43
M_DATA_A44	AR38	SA_MA_44
M_DATA_A45	AN38	SA_MA_45
M_DATA_A46	AN40	SA_MA_46
M_DATA_A47	AL40	SA_MA_47
M_DATA_A48	AL37	SA_MA_48
M_DATA_A49	AJ38	SA_MA_49
M_DATA_A50	AJ37	SA_MA_50
M_DATA_A51	AJ38	SA_MA_51
M_DATA_A52	AJ37	SA_MA_52
M_DATA_A53	AJ38	SA_MA_53
M_DATA_A54	AJ39	SA_MA_54
M_DATA_A55	AJ40	SA_MA_55
M_DATA_A56	AG40	SA_MA_56
M_DATA_A57	AG37	SA_MA_57
M_DATA_A58	AE38	SA_MA_58
M_DATA_A59	AE37	SA_MA_59
M_DATA_A60	AG39	SA_MA_60
M_DATA_A61	AG38	SA_MA_61
M_DATA_A62	AE39	SA_MA_62
M_DATA_A63	AE40	SA_MA_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7

M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV38	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

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SM\_DRAMRST#

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SA\_DQS#\_8

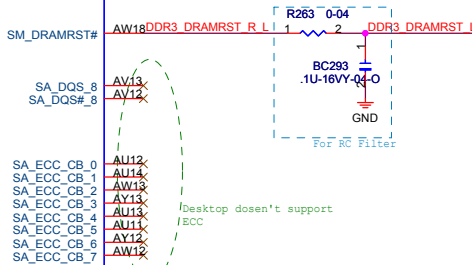
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SA\_ECC\_CB\_5  
SA\_ECC\_CB\_6  
SA\_ECC\_CB\_7

DDR\_0

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DDR3 CH.A



Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B8	AL7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B11	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B13	AL9	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B15	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AR7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AR9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B49	AM31	SB_DQ_49
M_DATA_B50	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B52	AM34	SB_DQ_52
M_DATA_B53	AM35	SB_DQ_53
M_DATA_B54	AL34	SB_DQ_54
M_DATA_B55	AL34	SB_DQ_55
M_DATA_B56	AH35	SB_DQ_56
M_DATA_B57	AH34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
M_DATA_B60	AJ35	SB_DQ_60
M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN3	SB_DQS_3
M_DQS_B_P4	AN3	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

CPU10

BALLMAP\_REV=1.4

SB_DQ_0	AK24	M_MA_B0
SB_DQ_1	AM20	M_MA_B1
SB_DQ_2	AM19	M_MA_B2
SB_DQ_3	AK18	M_MA_B3
SB_DQ_4	AP19	M_MA_B4
SB_DQ_5	AP18	M_MA_B5
SB_DQ_6	AM18	M_MA_B6
SB_DQ_7	AL18	M_MA_B7
SB_DQ_8	AN18	M_MA_B8
SB_DQ_9	AY17	M_MA_B9
SB_DQ_10	AN23	M_MA_B10
SB_DQ_11	AU17	M_MA_B11
SB_DQ_12	AT18	M_MA_B12
SB_DQ_13	AR26	M_MA_B13
SB_DQ_14	AY16	M_MA_B14
SB_DQ_15	AV16	M_MA_B15
SB_DQ_16	AR25	M_WE_B_L
SB_DQ_17	AK25	M_CAS_B_L
SB_DQ_18	AP24	M_RAS_B_L
SB_DQ_19	AP23	M_BS_B0
SB_DQ_20	AM24	M_BS_B1
SB_DQ_21	AW17	M_BS_B2
SB_DQ_22	AN25	M_CS_B_L0
SB_DQ_23	AN26	M_CS_B_L1
SB_DQ_24	AT25	M_CS_B_L2
SB_DQ_25	AT26	M_CS_B_L3
SB_DQ_26	AU16	M_CKE_B0
SB_DQ_27	AW15	M_CKE_B2
SB_DQ_28	AV15	M_CKE_B3
SB_DQ_29	AL26	M_ODT_B0
SB_DQ_30	AP26	M_ODT_B1
SB_DQ_31	AM26	M_ODT_B2
SB_DQ_32	AK26	M_ODT_B3
SB_DQ_33	AL21	M_CLK_B_P0
SB_DQ_34	AL22	M_CLK_B_N0
SB_DQ_35	AL20	M_CLK_B_P1
SB_DQ_36	AK20	M_CLK_B_N1
SB_DQ_37	AL23	M_CLK_B_P2
SB_DQ_38	AM22	M_CLK_B_N2
SB_DQ_39	AP21	M_CLK_B_P3
SB_DQ_40	AN21	M_CLK_B_N3

SB_DQS_8	AN18	M_MA_B8
SB_DQS#_8	AN15	M_MA_B5
SB_ECC_CB_0	AL16	M_MA_B6
SB_ECC_CB_1	AM16	M_MA_B7
SB_ECC_CB_2	AP16	M_MA_B8
SB_ECC_CB_3	AR16	M_MA_B9
SB_ECC_CB_4	AL15	M_MA_B10
SB_ECC_CB_5	AM15	M_MA_B11
SB_ECC_CB_6	AR15	M_MA_B12
SB_ECC_CB_7	AR15	M_MA_B13

DDR\_1

4 OF 10

LGA-1155P-S

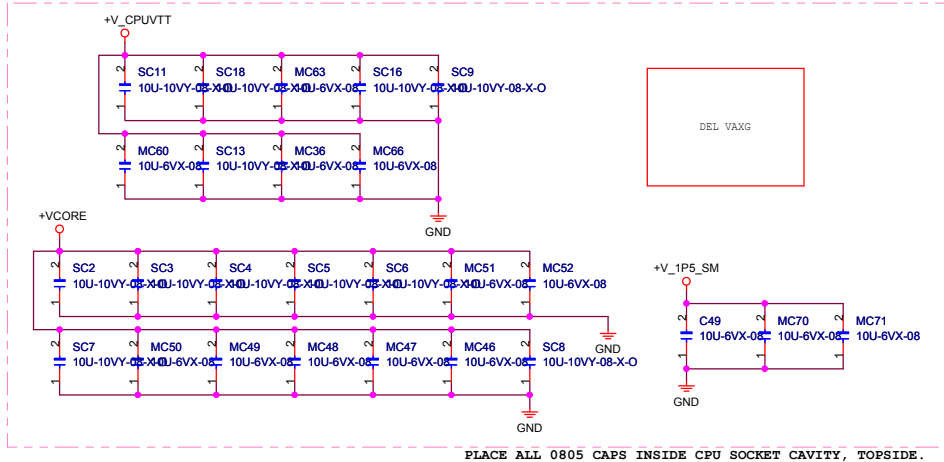
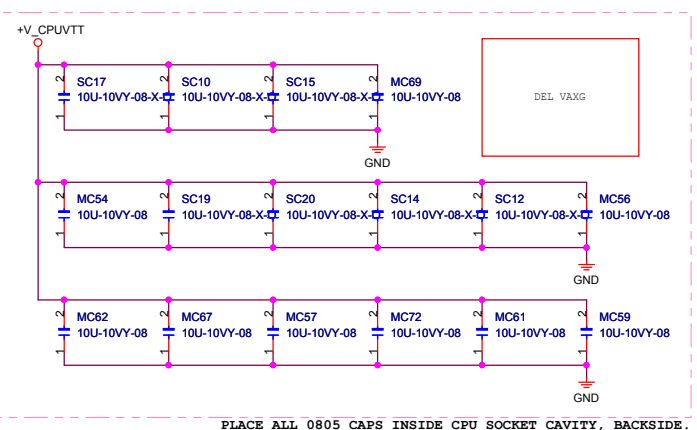
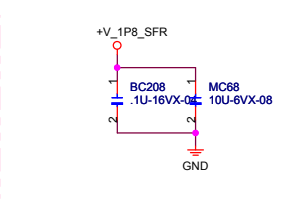
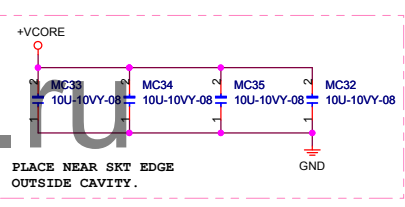
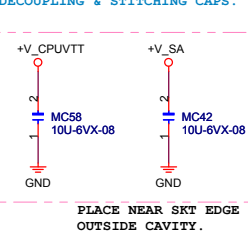
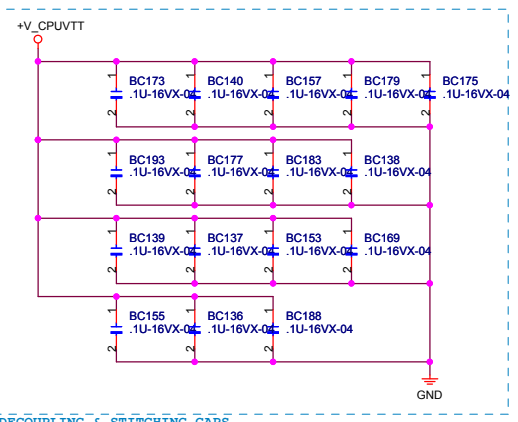
DDR3 CH.B

MAX 112A		MAX 112A	
In	+V_CORE	In	+V_CORE
A12	VCC_001	F32	VCC_082
A13	VCC_002	F33	VCC_083
A14	VCC_003	F34	VCC_084
A15	VCC_004	G15	VCC_085
A16	VCC_005	G16	VCC_086
A17	VCC_006	G17	VCC_087
A18	VCC_007	G18	VCC_088
A19	VCC_008	G19	VCC_089
A20	VCC_009	G20	VCC_090
A21	VCC_010	G21	VCC_091
A22	VCC_011	G22	VCC_092
A23	VCC_012	G23	VCC_093
A24	VCC_013	G24	VCC_094
A25	VCC_014	G25	VCC_095
A26	VCC_015	G26	VCC_096
A27	VCC_016	G27	VCC_097
A28	VCC_017	G28	VCC_098
A29	VCC_018	G29	VCC_099
A30	VCC_019	G30	VCC_100
A31	VCC_020	G31	VCC_101
A32	VCC_021	G32	VCC_102
A33	VCC_022	G33	VCC_103
A34	VCC_023	H13	VCC_104
A35	VCC_024	H14	VCC_105
A36	VCC_025	H15	VCC_106
A37	VCC_026	H16	VCC_107
A38	VCC_027	H17	VCC_108
A39	VCC_028	H18	VCC_109
A40	VCC_029	H19	VCC_110
A41	VCC_030	H20	VCC_111
A42	VCC_031	H21	VCC_112
A43	VCC_032	H22	VCC_113
A44	VCC_033	H23	VCC_114
A45	VCC_034	H24	VCC_115
A46	VCC_035	H25	VCC_116
A47	VCC_036	H26	VCC_117
A48	VCC_037	H27	VCC_118
A49	VCC_038	H28	VCC_119
A50	VCC_039	H29	VCC_120
A51	VCC_040	H30	VCC_121
A52	VCC_041	H31	VCC_122
A53	VCC_042	H32	VCC_123
A54	VCC_043	H33	VCC_124
A55	VCC_044	H34	VCC_125
A56	VCC_045	H35	VCC_126
A57	VCC_046	H36	VCC_127
A58	VCC_047	H37	VCC_128
A59	VCC_048	H38	VCC_129
A60	VCC_049	H39	VCC_130
A61	VCC_050	H40	VCC_131
A62	VCC_051	H41	VCC_132
A63	VCC_052	H42	VCC_133
A64	VCC_053	H43	VCC_134
A65	VCC_054	H44	VCC_135
A66	VCC_055	H45	VCC_136
A67	VCC_056	H46	VCC_137
A68	VCC_057	H47	VCC_138
A69	VCC_058	H48	VCC_139
A70	VCC_059	H49	VCC_140
A71	VCC_060	H50	VCC_141
A72	VCC_061	H51	VCC_142
A73	VCC_062	H52	VCC_143
A74	VCC_063	H53	VCC_144
A75	VCC_064	H54	VCC_145
A76	VCC_065	H55	VCC_146
A77	VCC_066	H56	VCC_147
A78	VCC_067	H57	VCC_148
A79	VCC_068	H58	VCC_149
A80	VCC_069	H59	VCC_150
A81	VCC_070	H60	VCC_151
A82	VCC_071	H61	VCC_152
A83	VCC_072	H62	VCC_153
A84	VCC_073	H63	VCC_154
A85	VCC_074	H64	VCC_155
A86	VCC_075	H65	VCC_156
A87	VCC_076	H66	VCC_157
A88	VCC_077	H67	VCC_158
A89	VCC_078	H68	VCC_159
A90	VCC_079	H69	VCC_160
A91	VCC_080	H70	VCC_161

1.05V/1.00V MAX 8.5A		1.5V MAX 4.5A	
In	+V_CPUVTT	In	+V_1P5_SM
M13	VCCIO_34	A113	VCCIO_01
A11	VCCIO_01	A114	VCCIO_02
A7	VCCIO_02	A123	VCCIO_03
AA3	VCCIO_03	A124	VCCIO_04
AB8	VCCIO_04	AB20	VCCIO_05
AF8	VCCIO_05	AR21	VCCIO_06
AG33	VCCIO_06	AR22	VCCIO_07
AJ16	VCCIO_07	AR23	VCCIO_08
AJ17	VCCIO_08	AR24	VCCIO_09
AJ26	VCCIO_09	AU19	VCCIO_10
AJ28	VCCIO_10	AU27	VCCIO_11
AJ32	VCCIO_11	AU31	VCCIO_12
AK15	VCCIO_12	AV21	VCCIO_13
AK17	VCCIO_13	AV24	VCCIO_14
AK19	VCCIO_14	AV25	VCCIO_15
AK21	VCCIO_15	AV29	VCCIO_16
AK23	VCCIO_16	AV33	VCCIO_17
AK27	VCCIO_17	AW31	VCCIO_18
AK29	VCCIO_18	AY23	VCCIO_19
AK30	VCCIO_19	AY26	VCCIO_20
B9	VCCIO_20	AY28	VCCIO_21
D10	VCCIO_21		VCCIO_22
D6	VCCIO_22		VCCIO_23
E3	VCCIO_23		VCCIO_24
E4	VCCIO_24		VCCIO_25
G3	VCCIO_25		VCCIO_26
G4	VCCIO_26		VCCIO_27
J3	VCCIO_27		VCCIO_28
J4	VCCIO_28		VCCIO_29
J7	VCCIO_29		VCCIO_30
J8	VCCIO_30		VCCIO_31
L3	VCCIO_31		VCCIO_32
L4	VCCIO_32		VCCIO_33
L7	VCCIO_33		VCCIO_34
N3	VCCIO_34		VCCIO_35
N4	VCCIO_35		VCCIO_36
N7	VCCIO_36		VCCIO_37
R3	VCCIO_37		VCCIO_38
R4	VCCIO_38		VCCIO_39
R7	VCCIO_39		VCCIO_40
U3	VCCIO_40		VCCIO_41
U4	VCCIO_41		VCCIO_42
U7	VCCIO_42		VCCIO_43
V8	VCCIO_43		VCCIO_44
W3	VCCIO_44		VCCIO_45

1.05V/1.00V MAX 8.5A		1.5V MAX 4.5A	
In	+V_CPUVTT	In	+V_1P5_SM
M13	VCCIO_34	A113	VCCIO_01
A11	VCCIO_01	A114	VCCIO_02
A7	VCCIO_02	A123	VCCIO_03
AA3	VCCIO_03	A124	VCCIO_04
AB8	VCCIO_04	AB20	VCCIO_05
AF8	VCCIO_05	AR21	VCCIO_06
AG33	VCCIO_06	AR22	VCCIO_07
AJ16	VCCIO_07	AR23	VCCIO_08
AJ17	VCCIO_08	AR24	VCCIO_09
AJ26	VCCIO_09	AU19	VCCIO_10
AJ28	VCCIO_10	AU27	VCCIO_11
AJ32	VCCIO_11	AU31	VCCIO_12
AK15	VCCIO_12	AV21	VCCIO_13
AK17	VCCIO_13	AV24	VCCIO_14
AK19	VCCIO_14	AV25	VCCIO_15
AK21	VCCIO_15	AV29	VCCIO_16
AK23	VCCIO_16	AV33	VCCIO_17
AK27	VCCIO_17	AW31	VCCIO_18
AK29	VCCIO_18	AY23	VCCIO_19
AK30	VCCIO_19	AY26	VCCIO_20
B9	VCCIO_20	AY28	VCCIO_21
D10	VCCIO_21		VCCIO_22
D6	VCCIO_22		VCCIO_23
E3	VCCIO_23		VCCIO_24
E4	VCCIO_24		VCCIO_25
G3	VCCIO_25		VCCIO_26
G4	VCCIO_26		VCCIO_27
J3	VCCIO_27		VCCIO_28
J4	VCCIO_28		VCCIO_29
J7	VCCIO_29		VCCIO_30
J8	VCCIO_30		VCCIO_31
L3	VCCIO_31		VCCIO_32
L4	VCCIO_32		VCCIO_33
L7	VCCIO_33		VCCIO_34
N3	VCCIO_34		VCCIO_35
N4	VCCIO_35		VCCIO_36
N7	VCCIO_36		VCCIO_37
R3	VCCIO_37		VCCIO_38
R4	VCCIO_38		VCCIO_39
R7	VCCIO_39		VCCIO_40
U3	VCCIO_40		VCCIO_41
U4	VCCIO_41		VCCIO_42
U7	VCCIO_42		VCCIO_43
V8	VCCIO_43		VCCIO_44
W3	VCCIO_44		VCCIO_45

1.05V/1.00V MAX 8.5A		1.5V MAX 4.5A	
In	+V_CPUVTT	In	+V_1P5_SM
M13	VCCIO_34	A113	VCCIO_01
A11	VCCIO_01	A114	VCCIO_02
A7	VCCIO_02	A123	VCCIO_03
AA3	VCCIO_03	A124	VCCIO_04
AB8	VCCIO_04	AB20	VCCIO_05
AF8	VCCIO_05	AR21	VCCIO_06
AG33	VCCIO_06	AR22	VCCIO_07
AJ16	VCCIO_07	AR23	VCCIO_08
AJ17	VCCIO_08	AR24	VCCIO_09
AJ26	VCCIO_09	AU19	VCCIO_10
AJ28	VCCIO_10	AU27	VCCIO_11
AJ32	VCCIO_11	AU31	VCCIO_12
AK15	VCCIO_12	AV21	VCCIO_13
AK17	VCCIO_13	AV24	VCCIO_14
AK19	VCCIO_14	AV25	VCCIO_15
AK21	VCCIO_15	AV29	VCCIO_16
AK23	VCCIO_16	AV33	VCCIO_17
AK27	VCCIO_17	AW31	VCCIO_18
AK29	VCCIO_18	AY23	VCCIO_19
AK30	VCCIO_19	AY26	VCCIO_20
B9	VCCIO_20	AY28	VCCIO_21
D10	VCCIO_21		VCCIO_22
D6	VCCIO_22		VCCIO_23
E3	VCCIO_23		VCCIO_24
E4	VCCIO_24		VCCIO_25
G3	VCCIO_25		VCCIO_26
G4	VCCIO_26		VCCIO_27
J3	VCCIO_27		VCCIO_28
J4	VCCIO_28		VCCIO_29
J7	VCCIO_29		VCCIO_30
J8	VCCIO_30		VCCIO_31
L3	VCCIO_31		VCCIO_32
L4	VCCIO_32		VCCIO_33
L7	VCCIO_33		VCCIO_34
N3	VCCIO_34		VCCIO_35
N4	VCCIO_35		VCCIO_36
N7	VCCIO_36		VCCIO_37
R3	VCCIO_37		VCCIO_38
R4	VCCIO_38		VCCIO_39
R7	VCCIO_39		VCCIO_40
U3	VCCIO_40		VCCIO_41
U4	VCCIO_41		VCCIO_42
U7	VCCIO_42		VCCIO_43
V8	VCCIO_43		VCCIO_44
W3	VCCIO_44		VCCIO_45



CHANG TO GND

VBALLMAP\_REV=1.4

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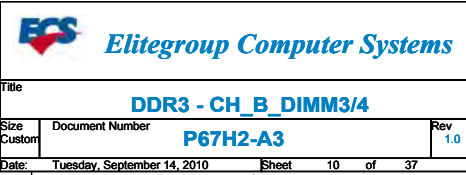
VCCAXG Core rail:  
Can connect this rail to ground  
if Mobo supports external graphics  
and if graphics VR is not stuffed.

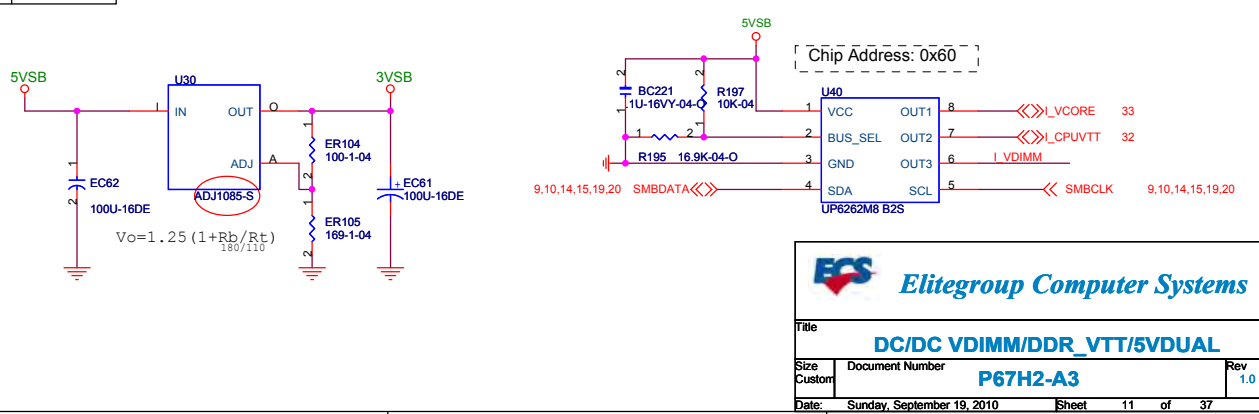
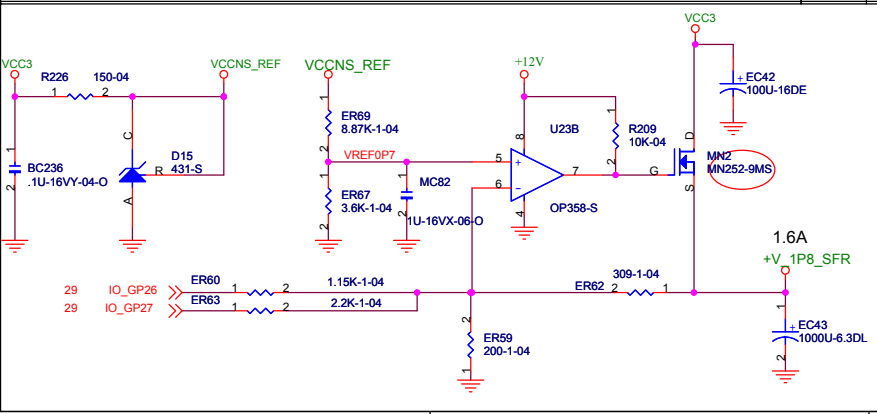
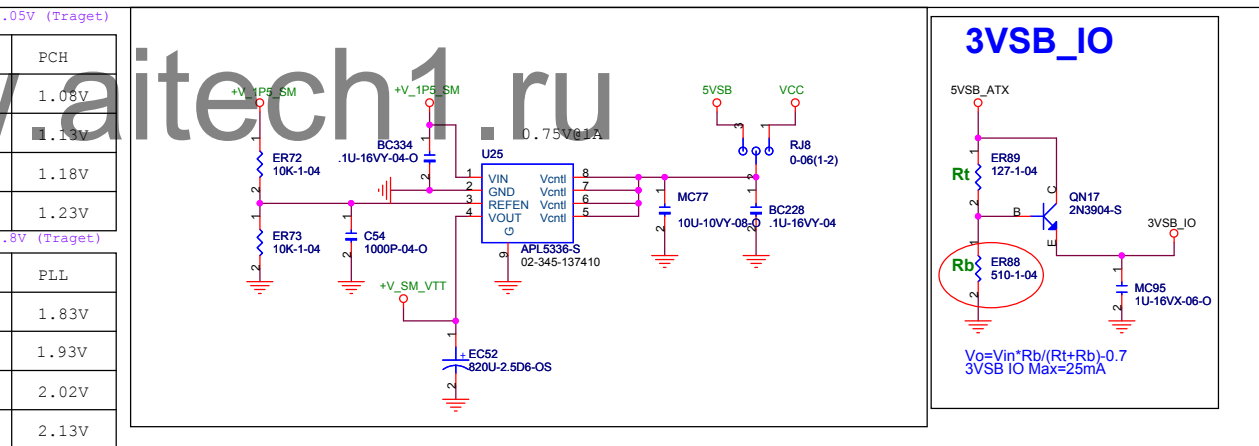
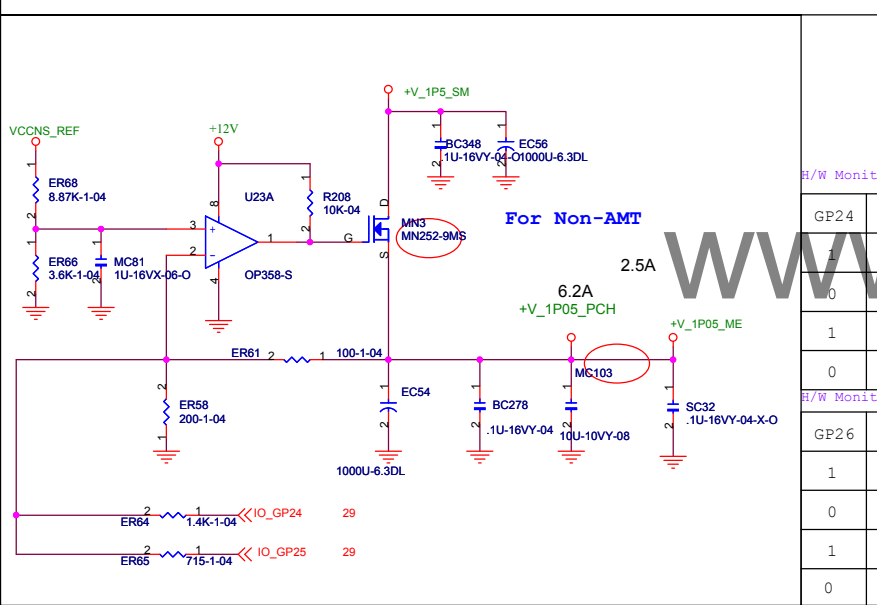
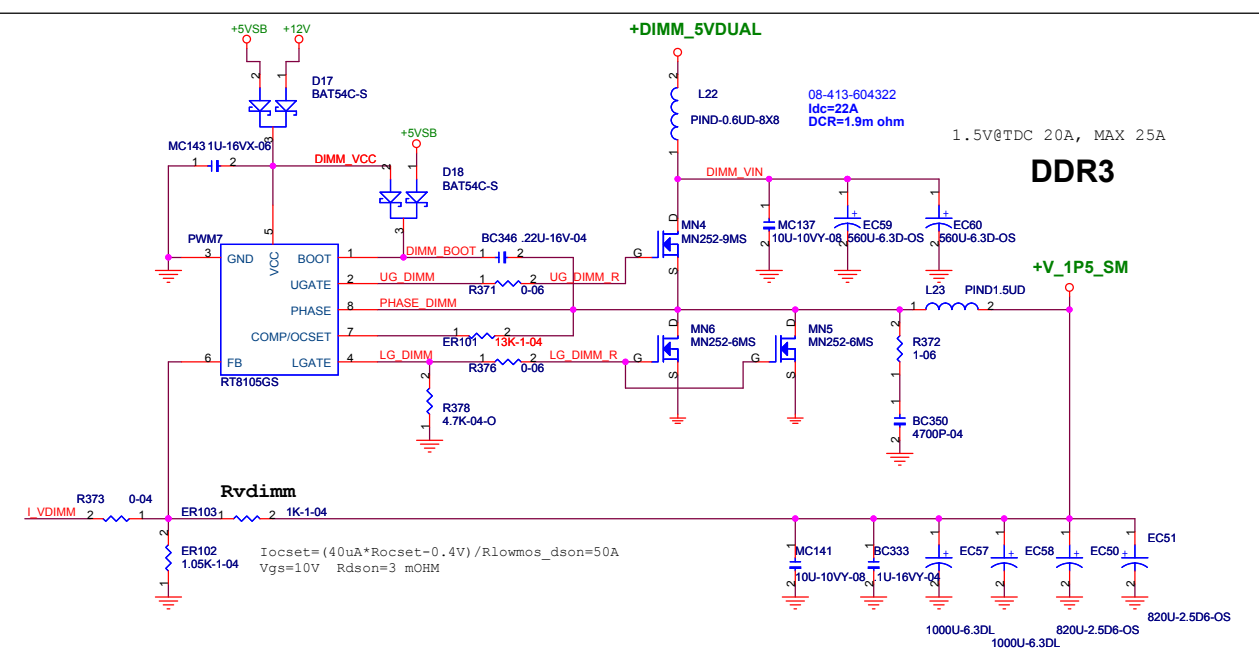
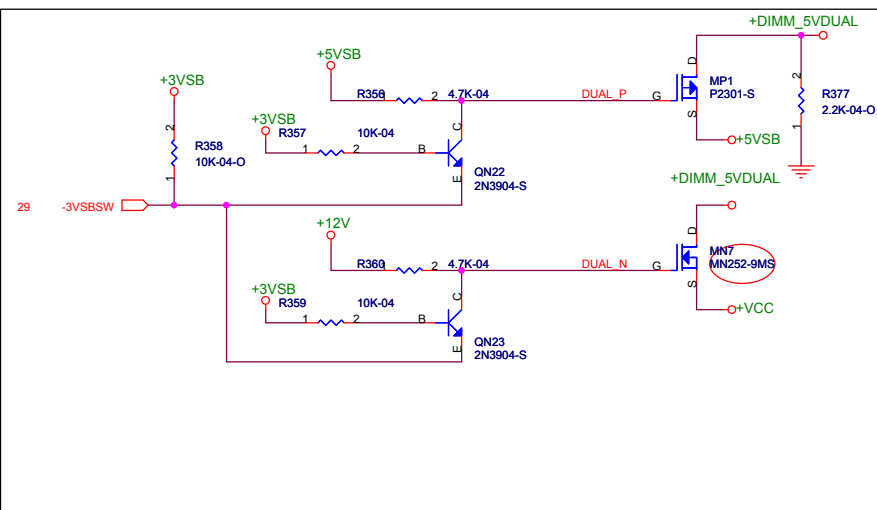
1



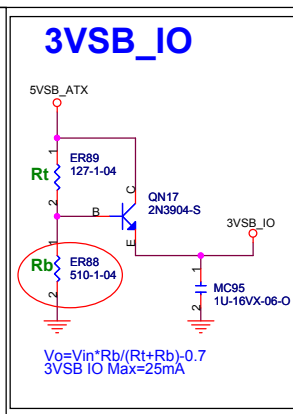






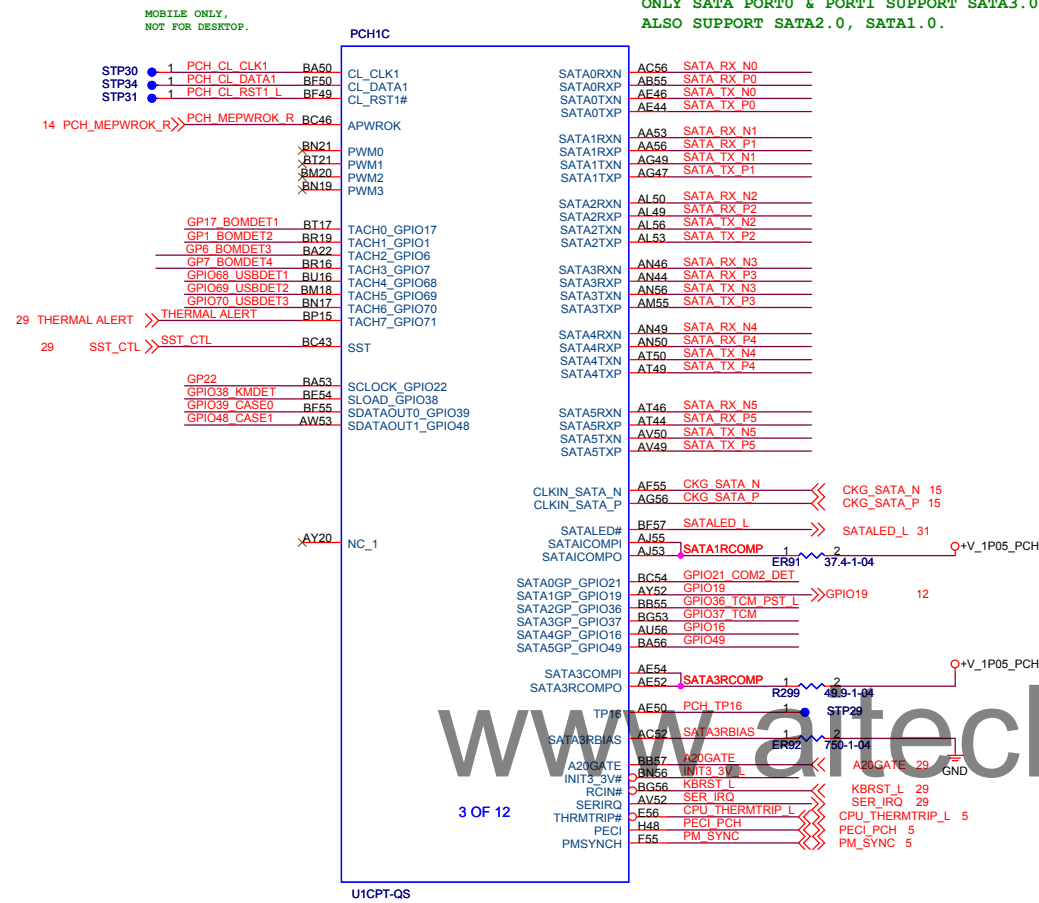


GP24	GP25	PCH
1	1	1.08V
0	1	1.18V
1	0	1.18V
0	0	1.23V
GP26	GP27	PLL
1	1	1.83V
0	1	1.93V
1	0	2.02V
0	0	2.13V





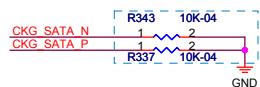
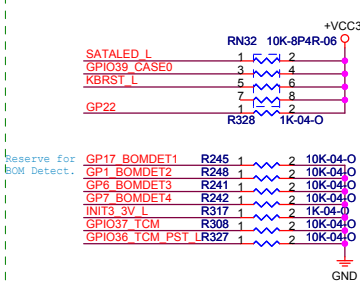
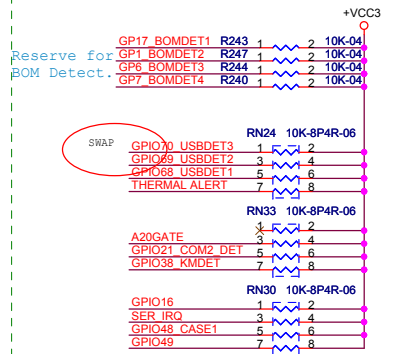




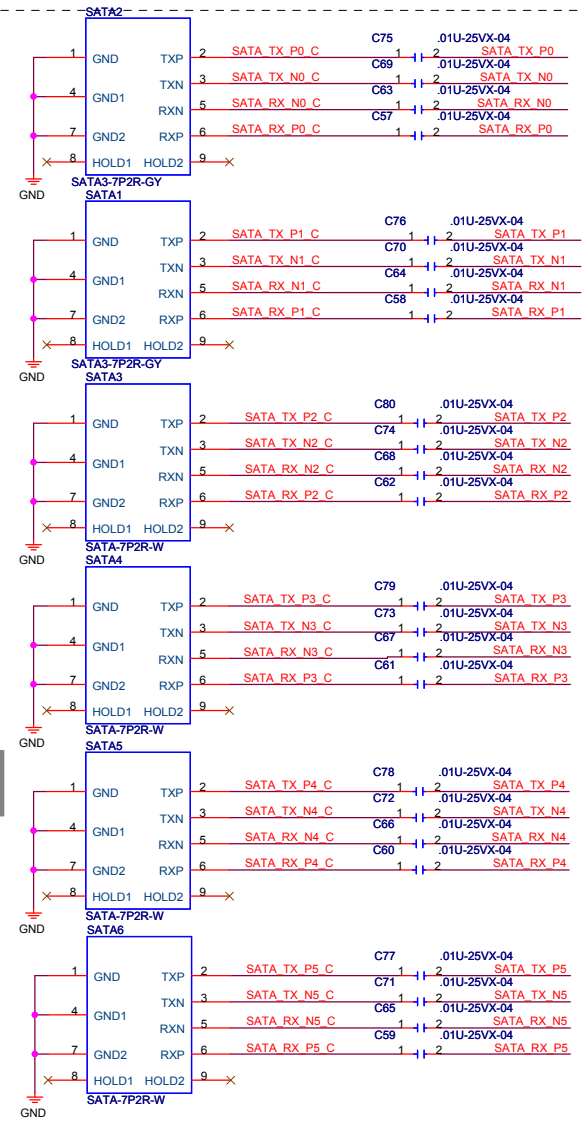
Default GPI set to Pull Up:

GPIO36\_TCM\_PST\_L, GPIO37\_TCM:  
TCM Reader In Enable TCM,  
Disable TPM.

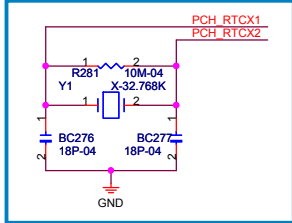
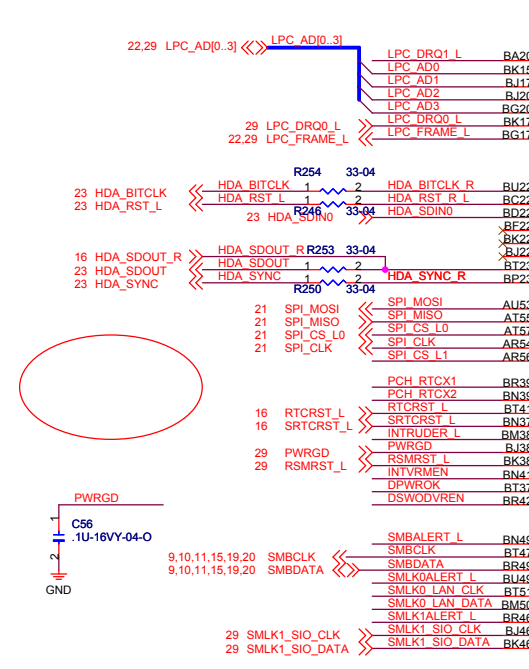
GPIO16, GPIO49:  
Reserve for TPM.



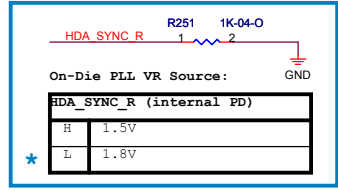
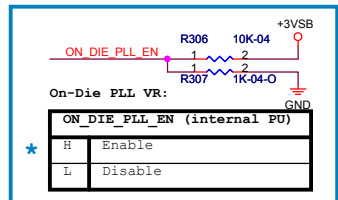
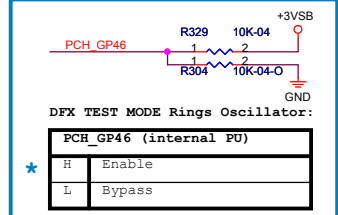
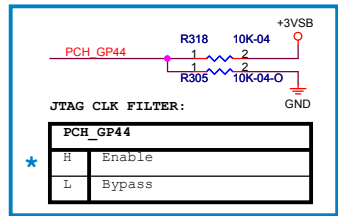
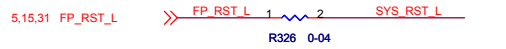
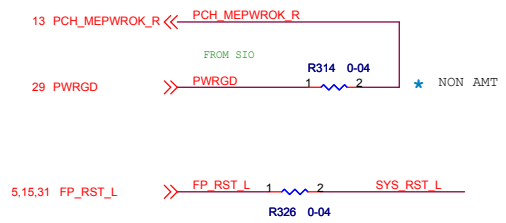
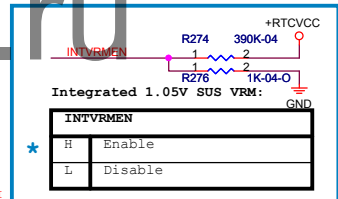
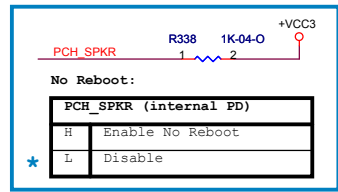
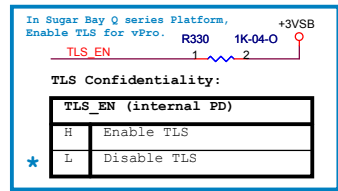
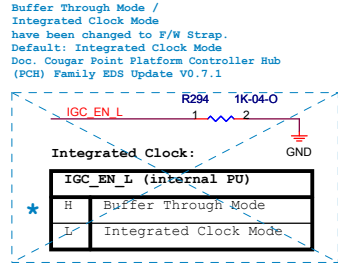
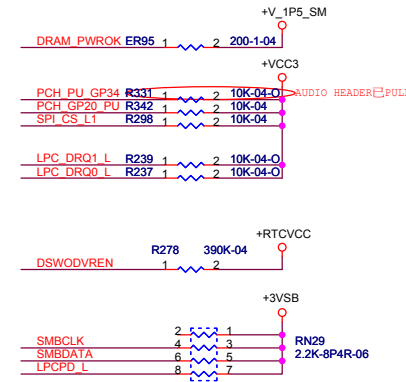
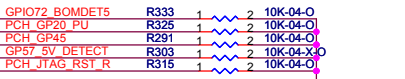
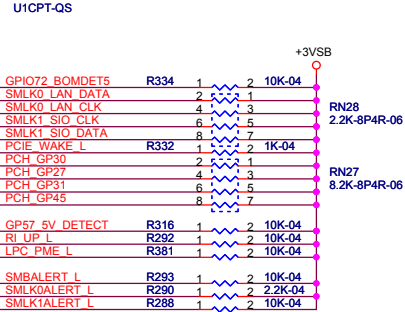
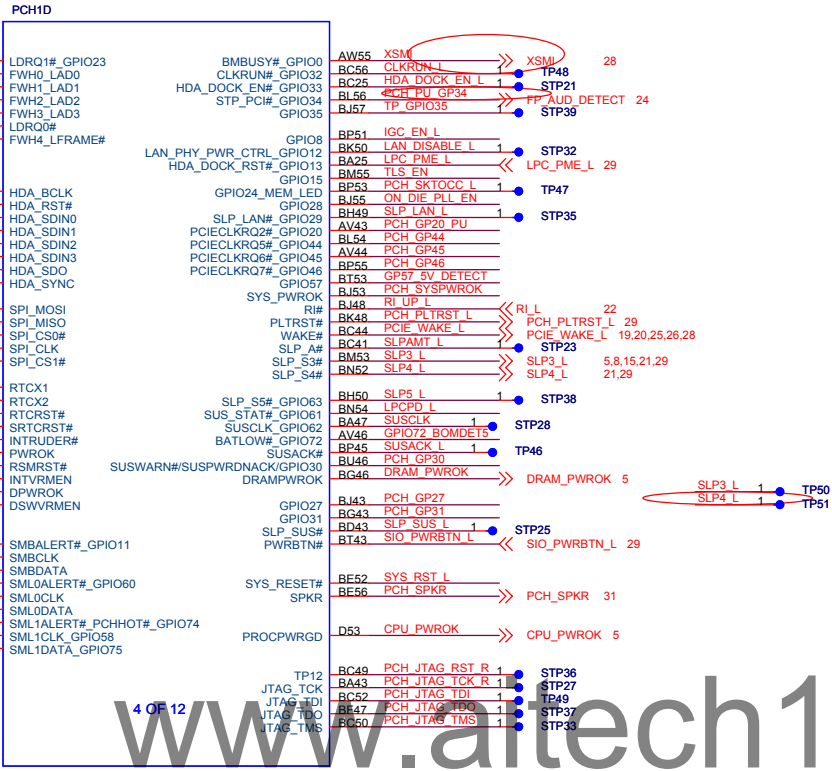
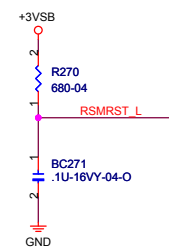
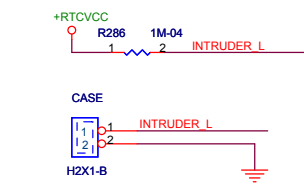
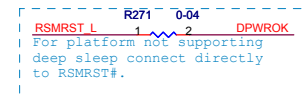
Stuff for Integrated Clock Mode



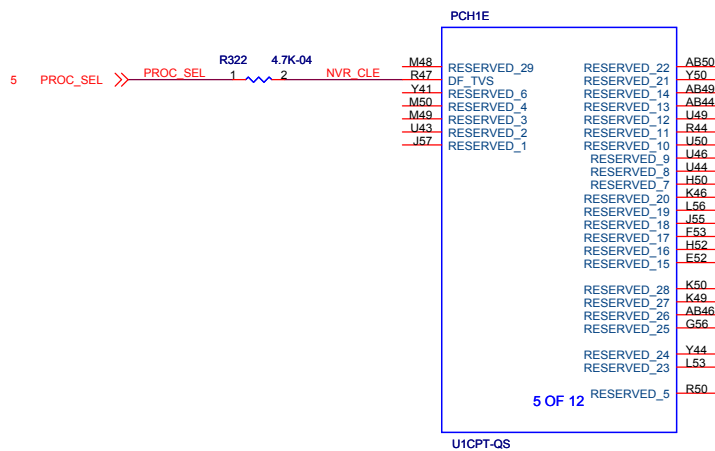
Layout Note:  
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%  
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%



When Deep Sleep not implemented:  
1. PCH\_GP30, PCH\_GP27 need to be Pull Up.  
2. VCCDSW3\_3 should to be connected to +3VSB.  
3. SLP\_SUS\_L, SUSACK\_L left unconnected.  
4. SUSWARN# may be used as GPIO30. (Reference to 1.)



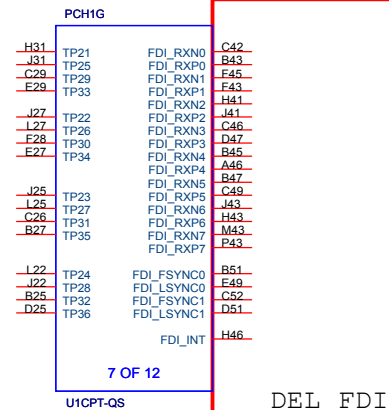




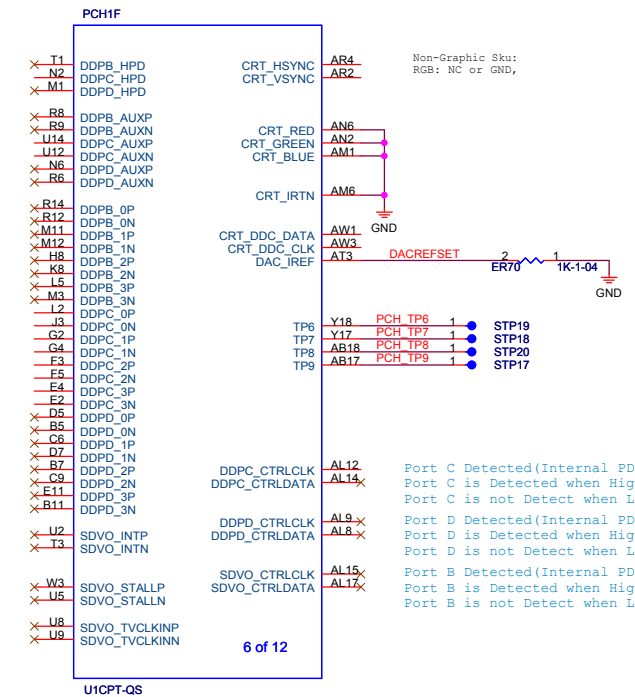
091222 Update!  
Terminating unused DC NAND interface:  
If not implemented, the dual channel NAND interface signals, including NV\_RCOMP, can be left as No Connect.

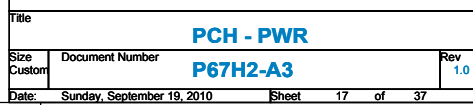
Note:  
VCCFNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

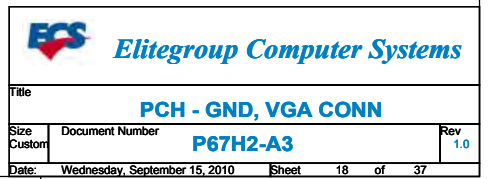
100120 Update!  
428880\_428880\_Cougar\_Point\_Desktop\_Ballout\_Mech\_Package\_Rev1p0.zip:  
Renamed NV\_WE#\_CK[0:1], NV\_RE#\_WRB[0:1], NV\_RCOMP, NV\_RB#, NV\_DQ9 / NV\_IO[0:15], NV\_DQS[0:1], NV\_CE#[0:3], and NV\_ALE to Reserved(RSVN).  
Renamed NV\_CLE to DF\_TVS.



7 OF 12  
U1CPT-QS  
DEL FDI

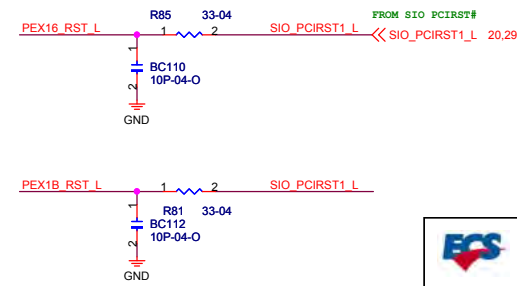
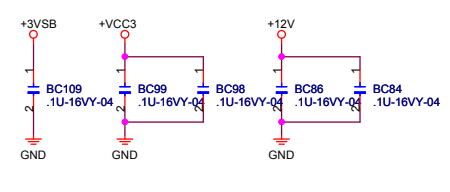
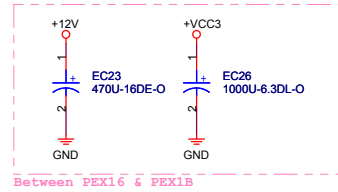
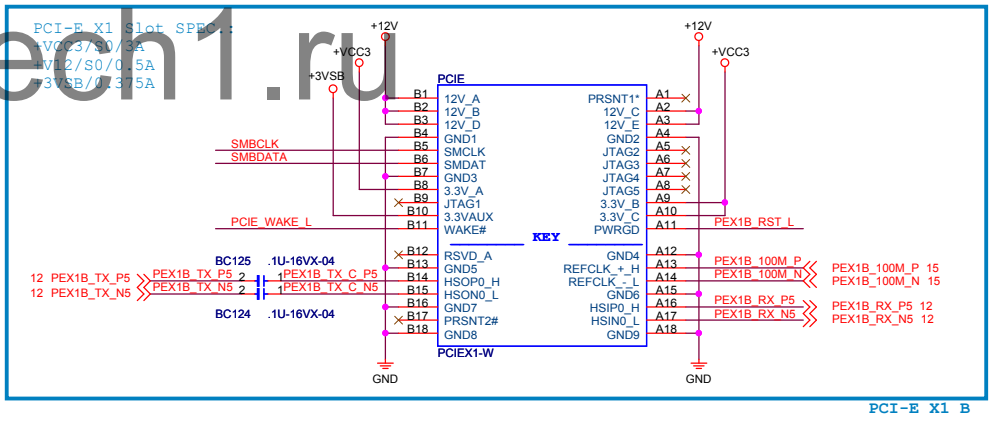
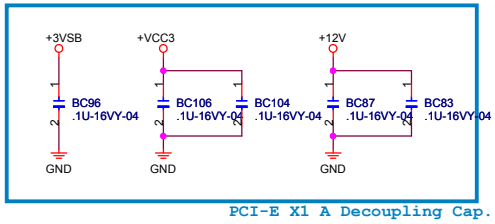
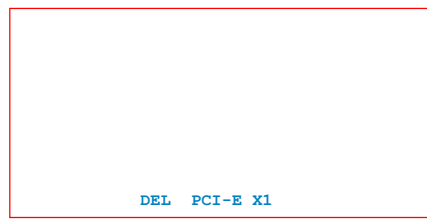
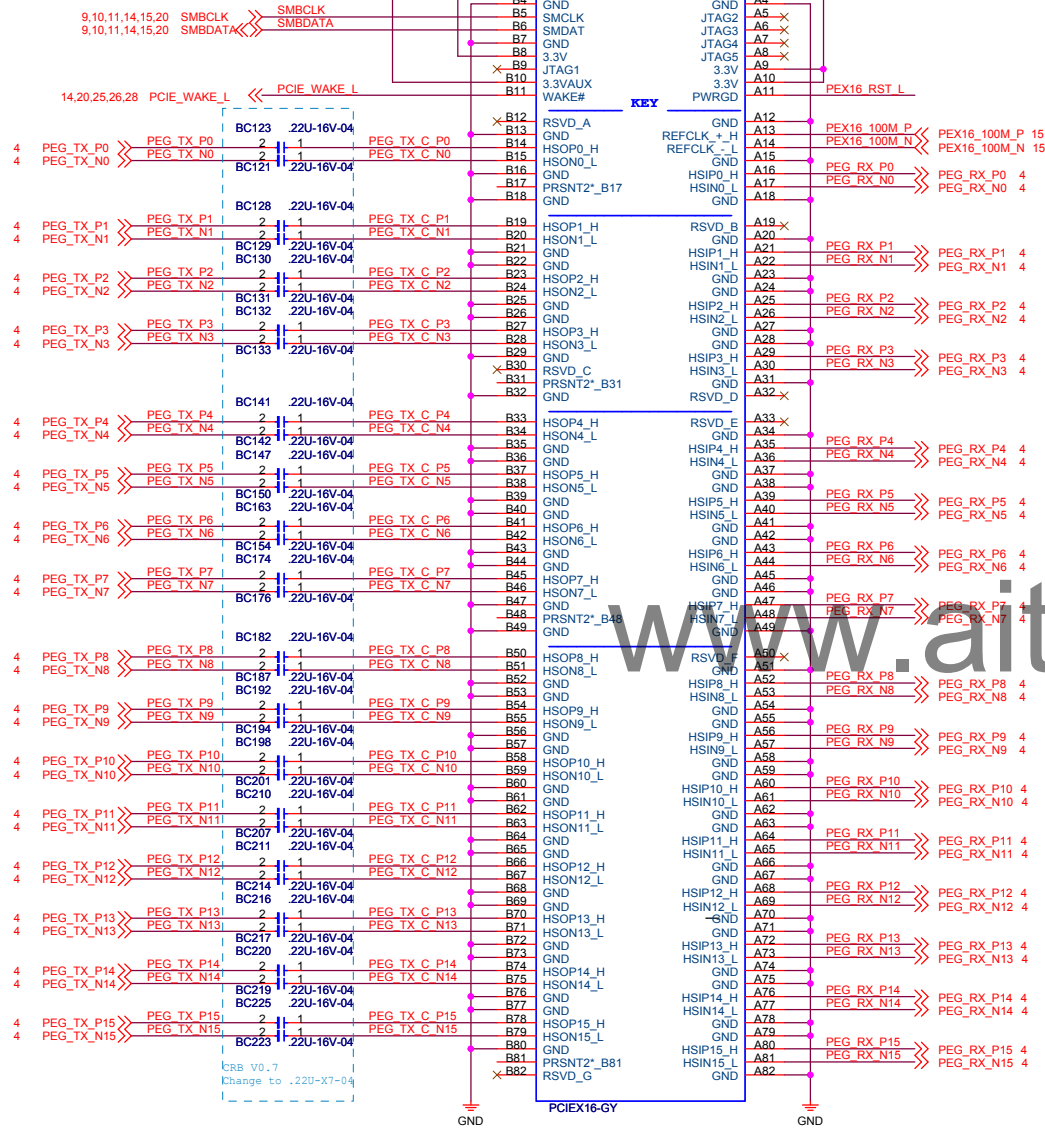








PCI-E X16 Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A

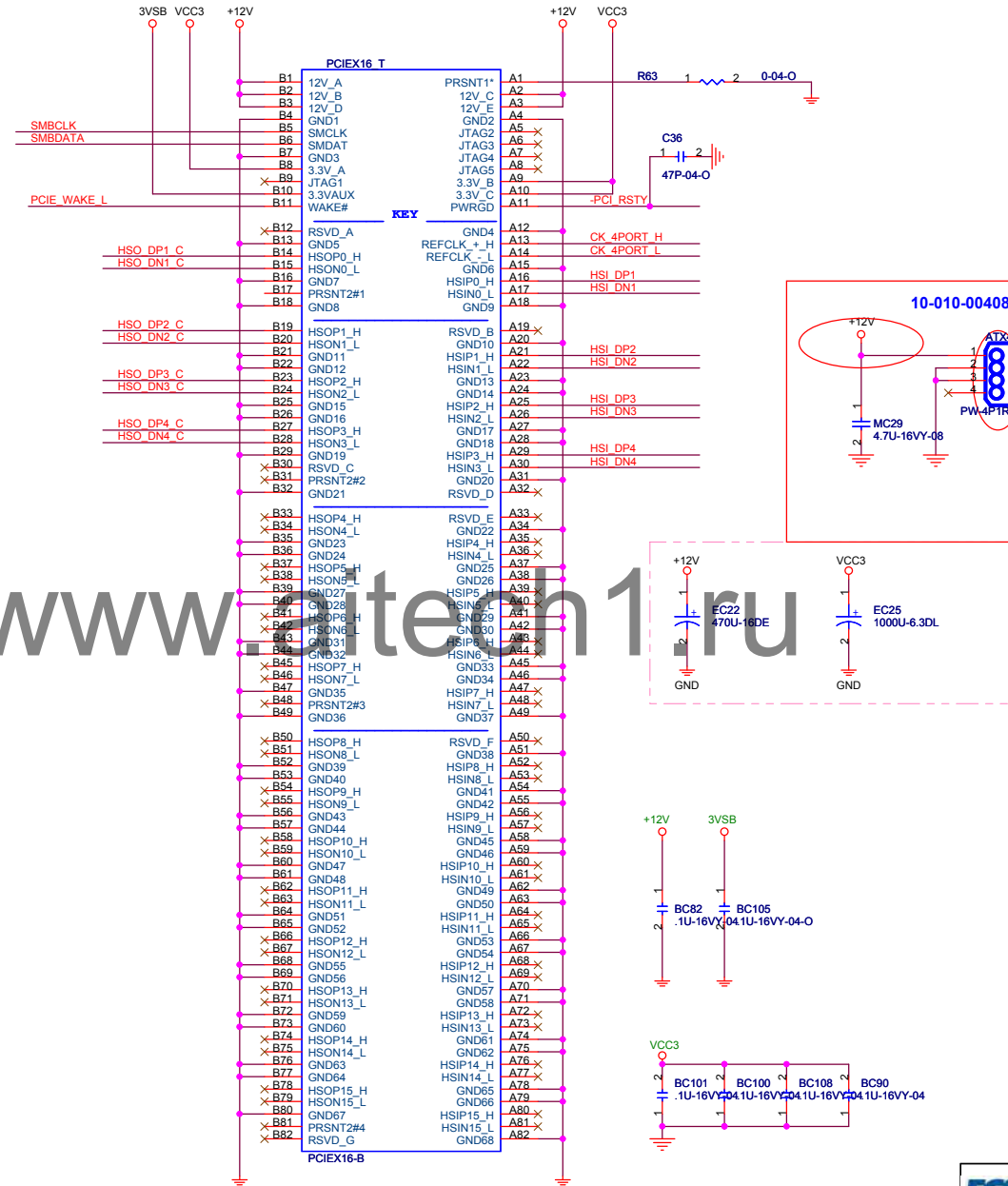


## External Connection



HSO DN1	C37	1	21U-16VX-04	HSO DN1 C
HSO DP1	C38	1	21U-16VX-04	HSO DP1 C
HSO DN2	C41	1	21U-16VX-04	HSO DN2 C
HSO DP2	C40	1	21U-16VX-04	HSO DP2 C
HSO DN3	C43	1	21U-16VX-04	HSO DN3 C
HSO DP3	C42	1	21U-16VX-04	HSO DP3 C
HSO DN4	C45	1	21U-16VX-04	HSO DN4 C
HSO DP4	C44	1	21U-16VX-04	HSO DP4 C

Near chipset

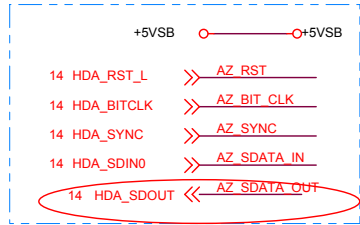




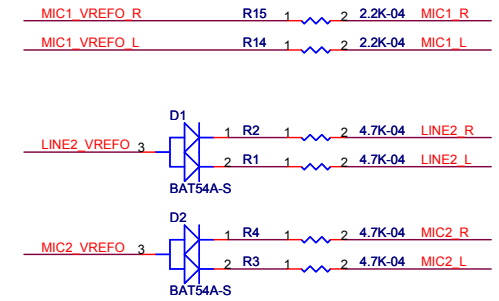




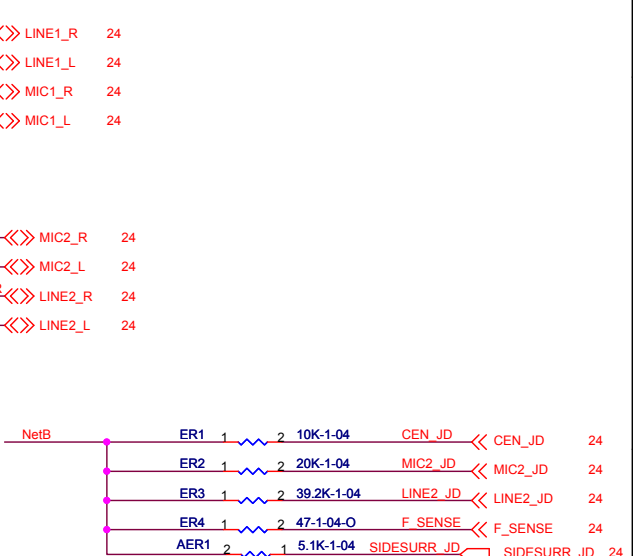
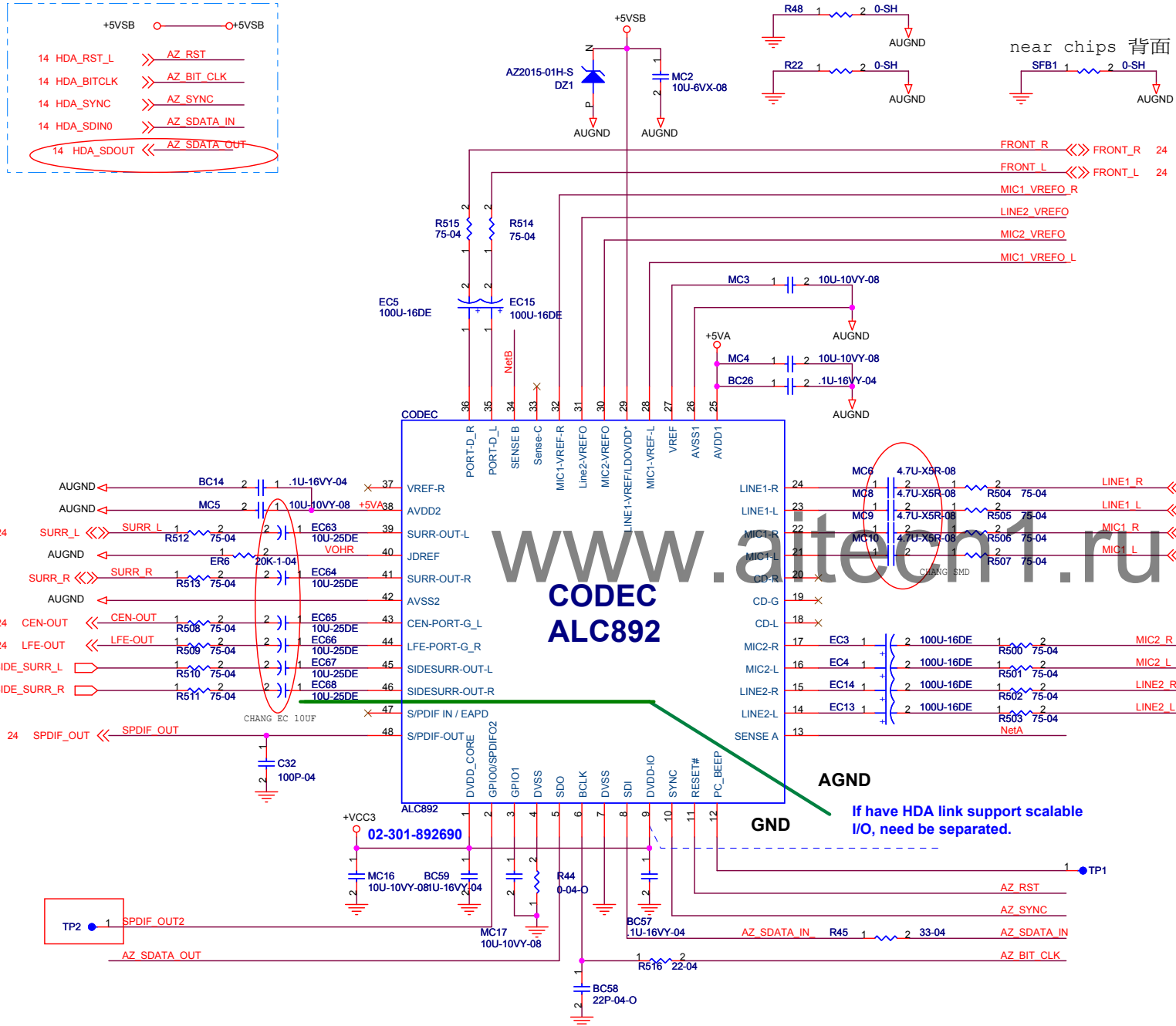
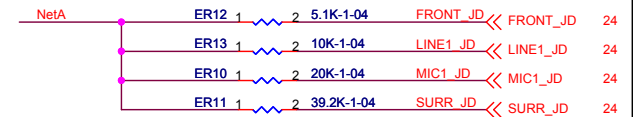
## External Connection



## Verfourt bias for stereo microphone.



## Place near codec Resistors Networks



Elitegroup Computer Systems

Title: Audio - ALC892

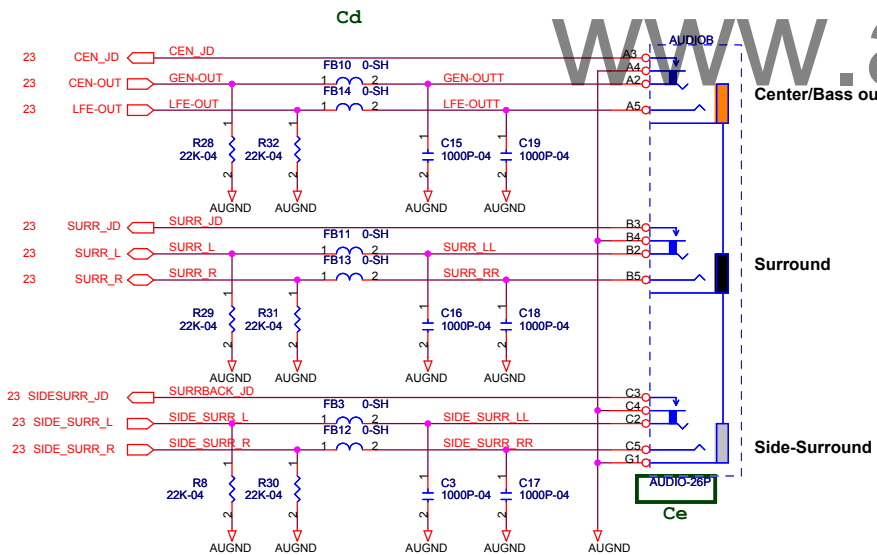
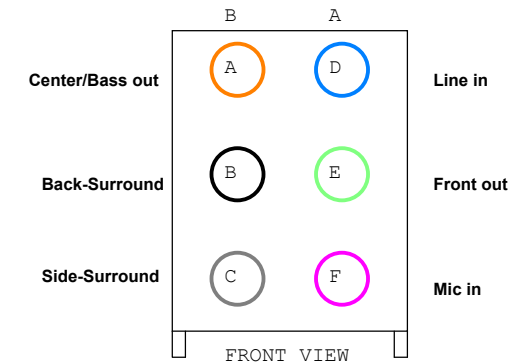
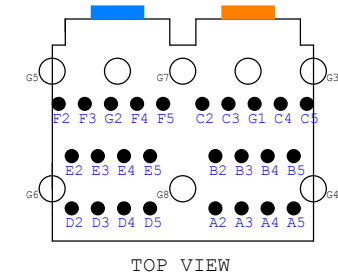
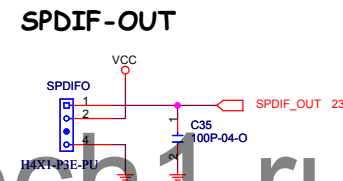
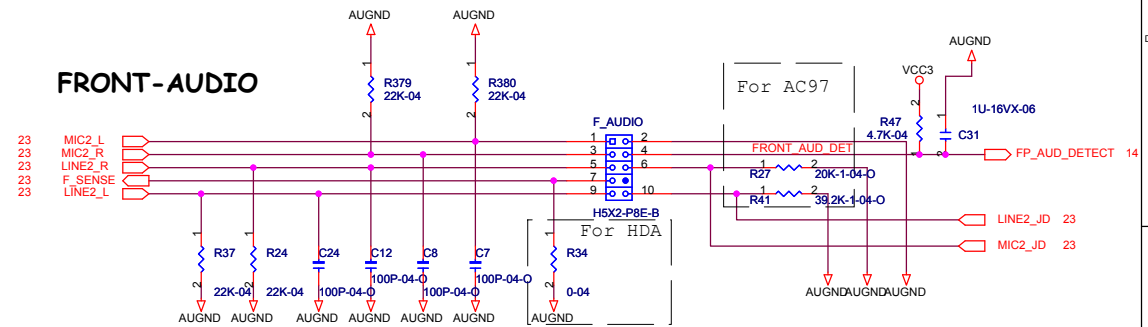
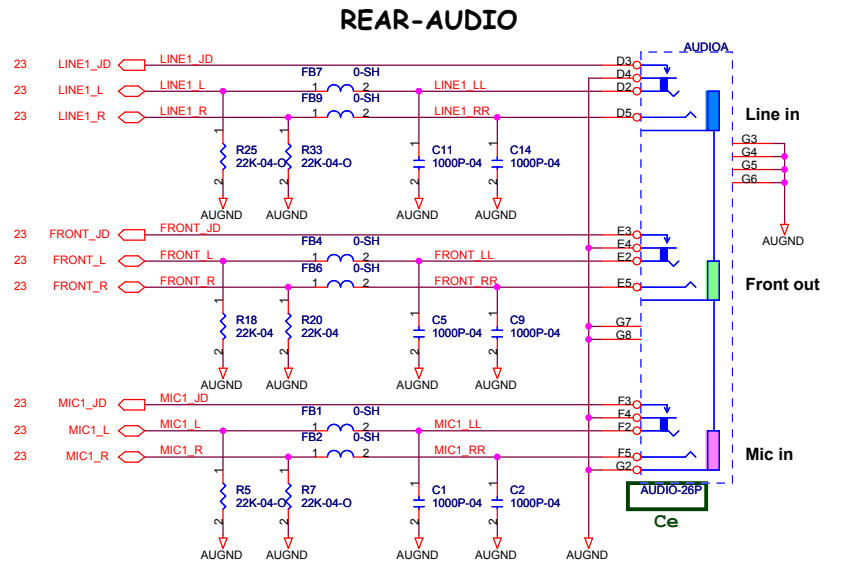
Size: Custom

Document Number: P67H2-A3

Date: Friday, September 17, 2010

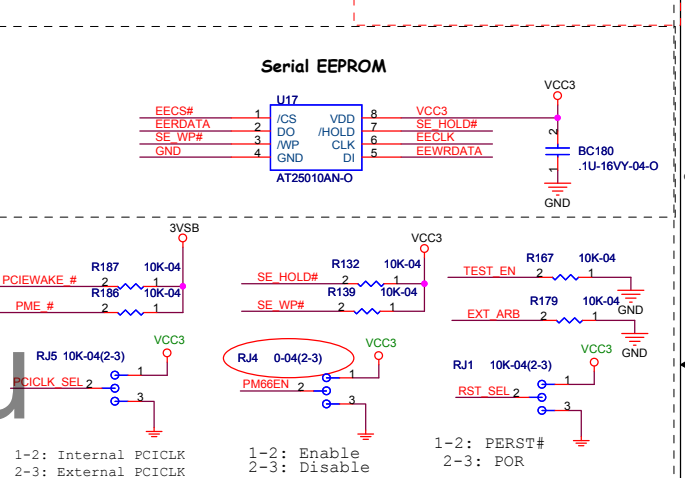
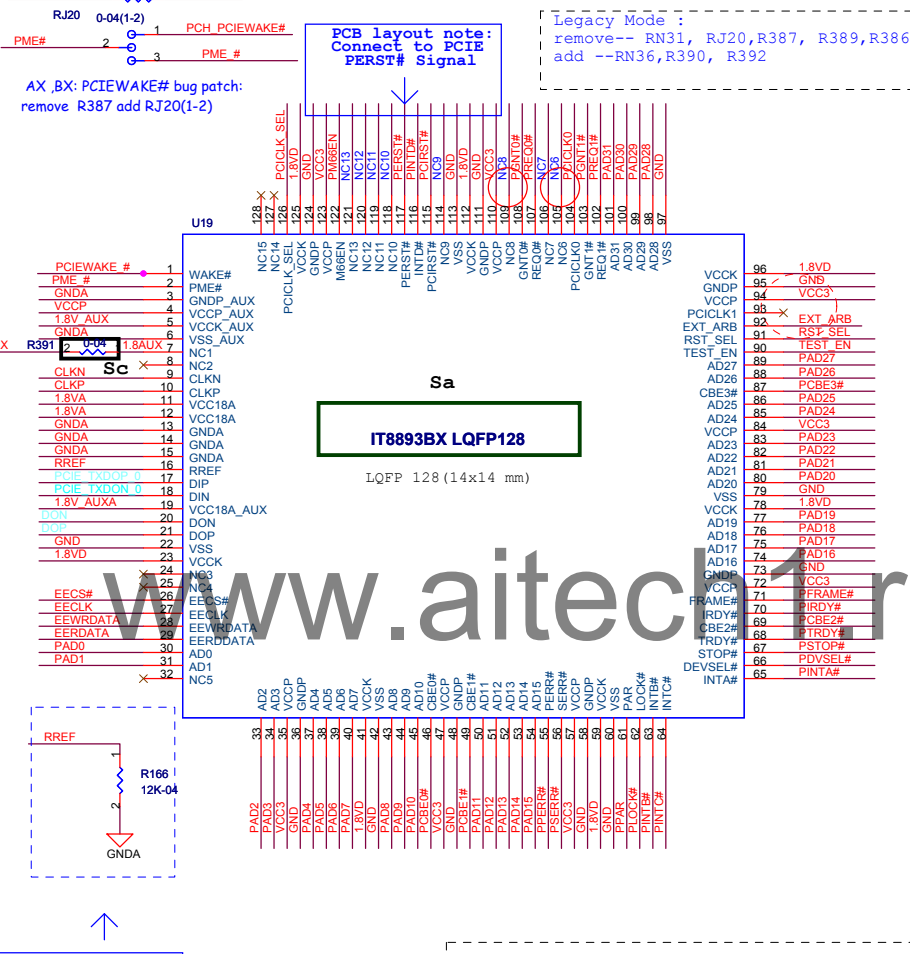
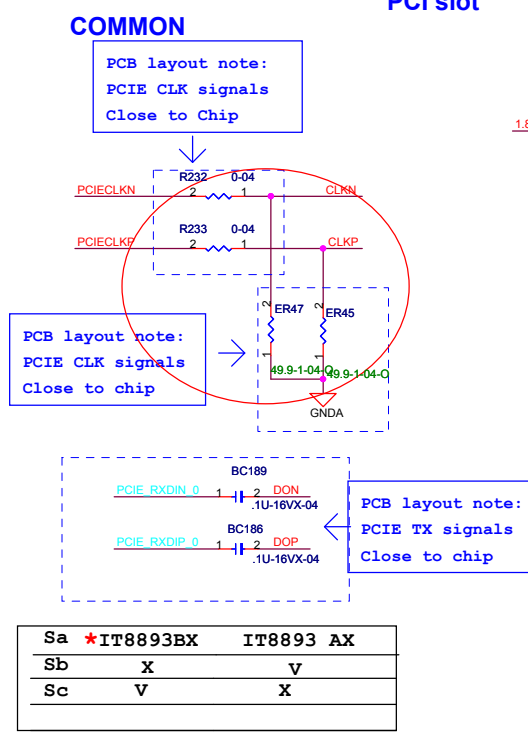
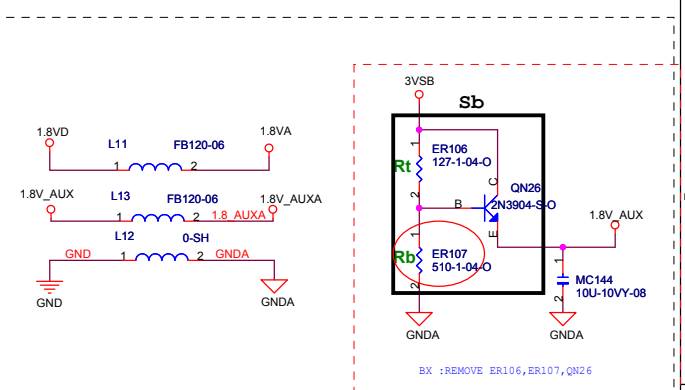
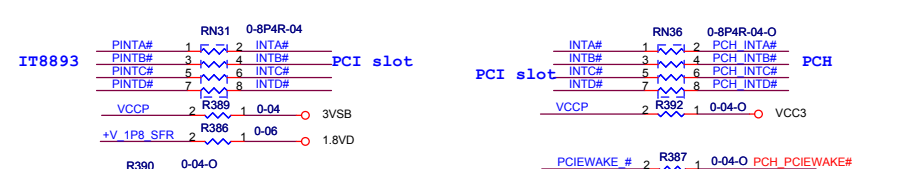
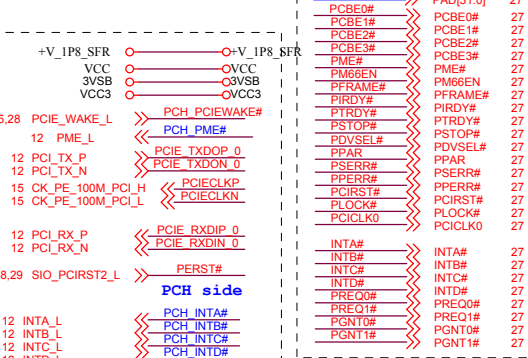
Sheet: 23 of 37

Rev: 1.0



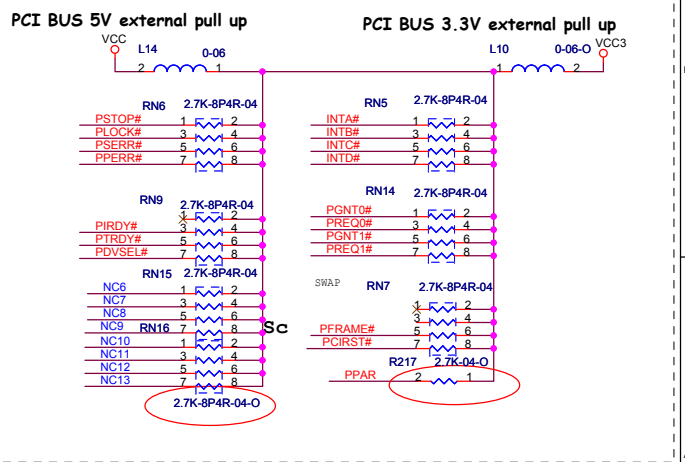


External Connection



PCIE DIP;DIN;DOP;DON PCB layout note:  
To meet Differential Impedance :85 ohm +/- 15%  
To meet Single-ended Impedance :50 ohm +/- 15%  
PCIE DIP and DIN trace width:9.5 mils  
PCIE DOP and DON trace width:9.5 mils  
Space between DIP/DIN and DOP/DON:14.5 mils  
L1 & L2 height:5 mils  
The signal traces Number of vias: 2 (Max.)  
The signal trace above analog GND plane  
Spacing from other groups:>25 mils  
Total trace length: 12 inches (Max.)

PCIE CLK PCB layout note:  
To meet Differential Impedance :100 ohm +/- 15%  
To meet Single-ended Impedance :50 ohm +/- 15%  
CLKP and CLKN trace width:7 mils  
Space between CLKP and CLKN:14 mils  
L1 & L2 height:5 mils  
The signal traces Number of vias: 4 (Max.)  
The signal trace above analog GND plane  
Spacing from other groups:>25 mils  
Total trace length: 12 inches (Max.)

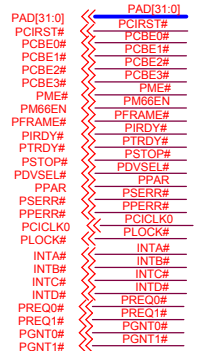




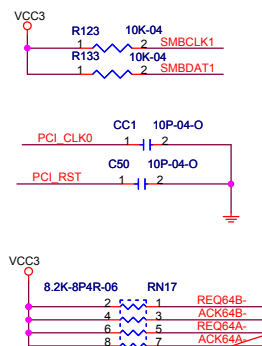
# External Connection



## COMMON

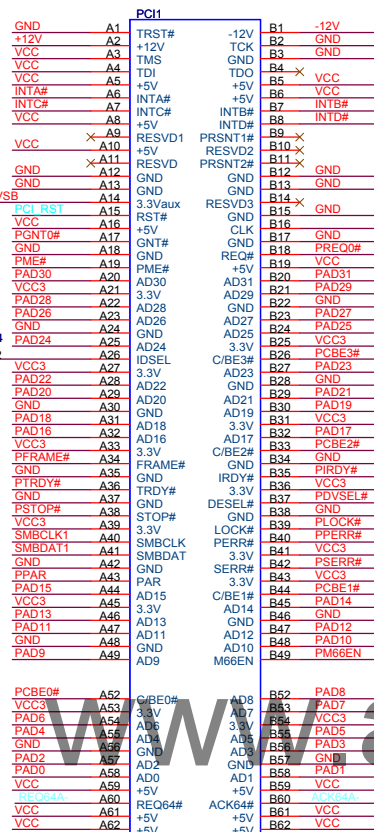


## PCI CHIP

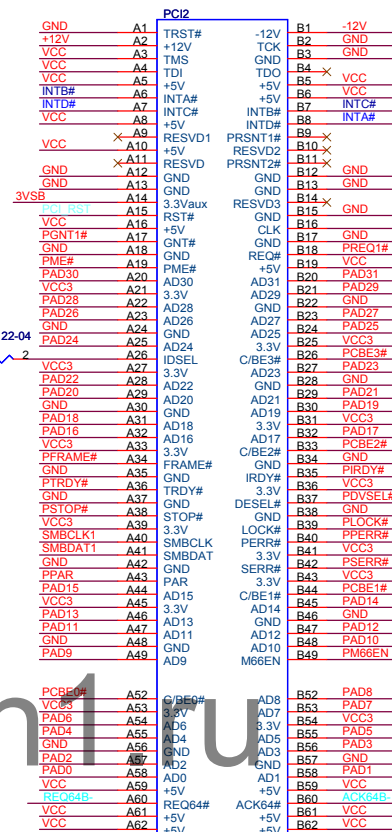


PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD  
PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA

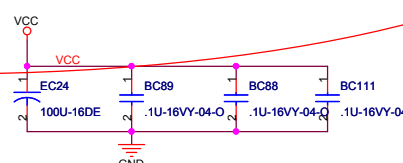
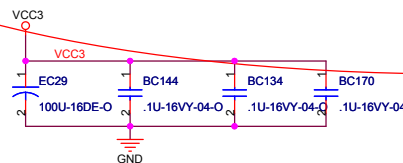
## PCI1



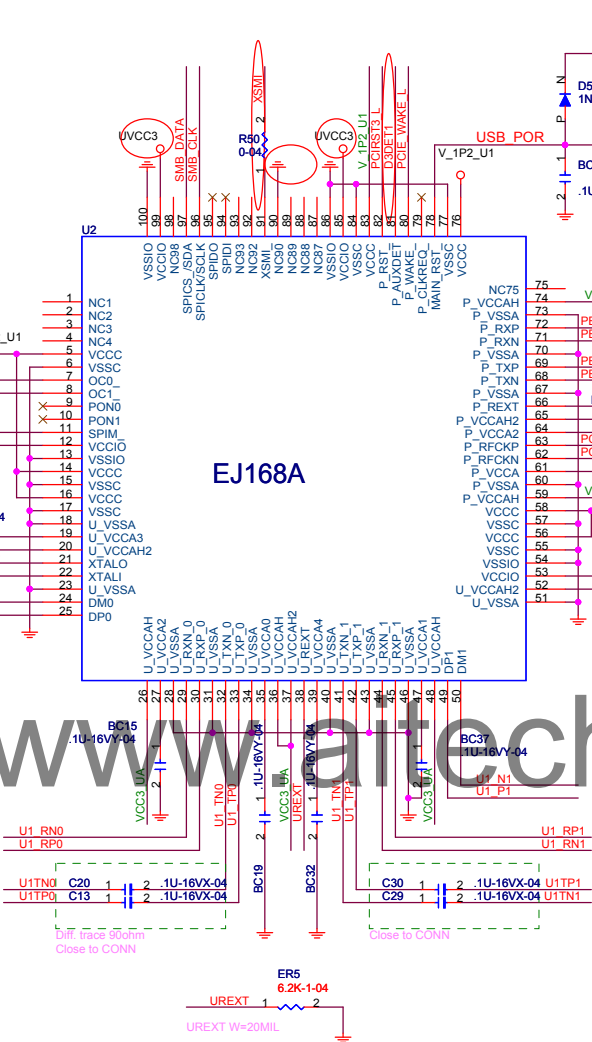
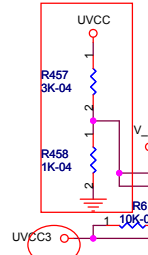
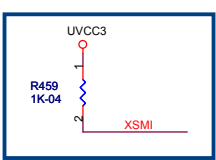
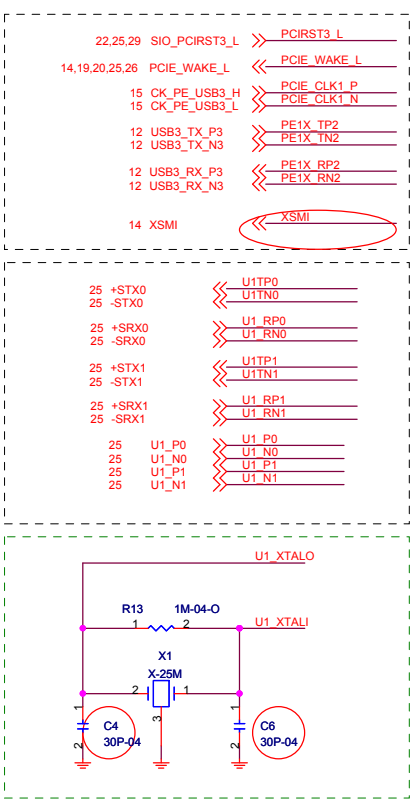
## PCI2



## 精簡零件



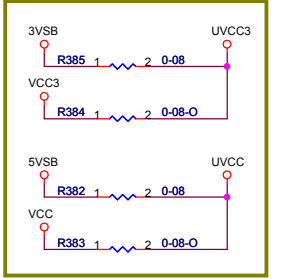
External Connection



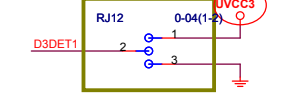
BOM Difference

	Wake up	No Wake up
U3a	RJ12 (1-2)	RJ12 (2-3)
U3b	R385, R382	R383, R384

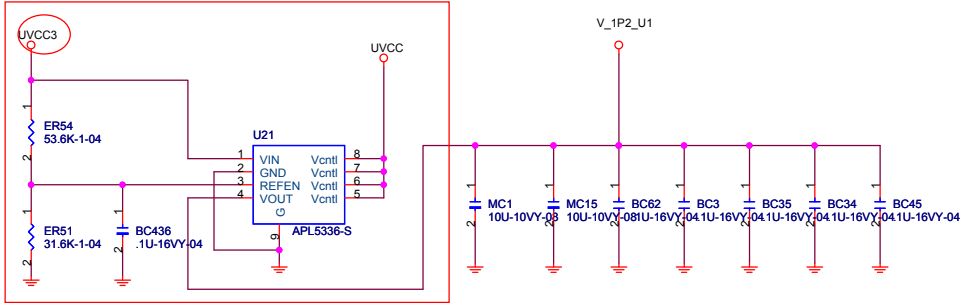
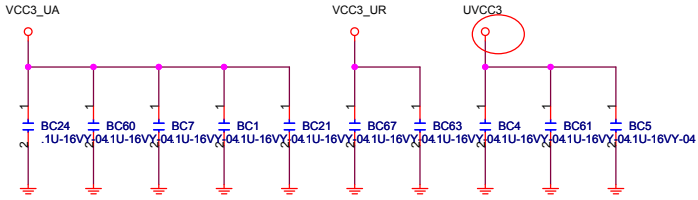
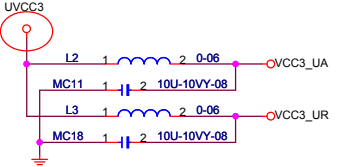
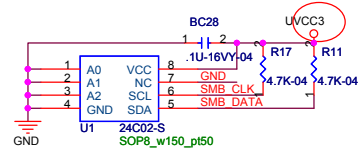
U3b



U3a



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www.aitech1.ru

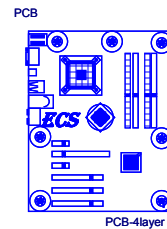
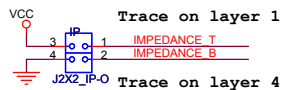
### 1)Circuit type 1

Layer 1:TOP

Layer 2:PWR

Layer 3:GND

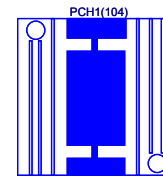
Layer 4:BOTTOM



PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

20-120-012343

MOS HK  
MOSFET HEATSINK



20-120-010851

PN:20-120-010851

CLR\_CMOS(1-2)



JP-R

BT(104)



CR2032

Y1(wire)

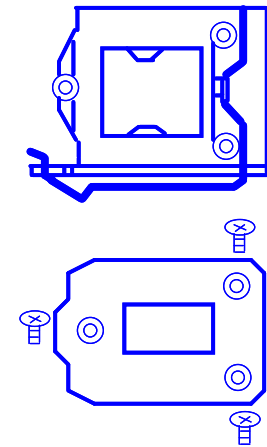


JP-WI-P6.25

11-018-115021 CPU SMD SOCKET  
SOCKET.CPU.LGA.1155P.SMD.BLACK.PE115527-4041-01F.  
LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL  
SUBASSY.STEEL.LGA.1156P.W/  
BACK PLATE.PT44A11-6401.LEAD-FREE(RoHS).FOXCONN

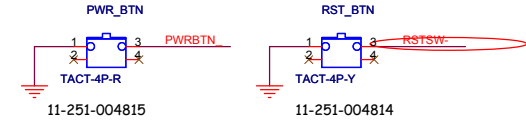
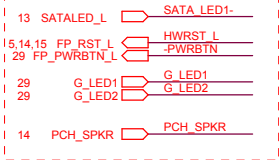
CPU1(104)  
CPU\_SUBASSY\_STEEL



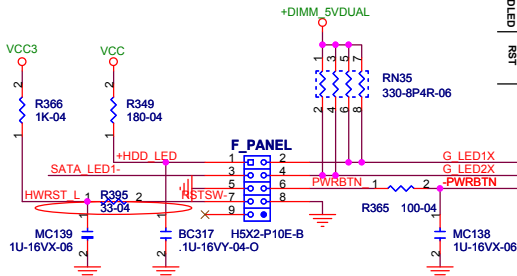
01D201-000060 PCH ES0

Title		
Size	Document Number	Rev
Custom	P67H2-A3	1.0
Date:	Thursday, September 23, 2010	Sheet 30 of 37

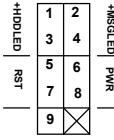
External Connection



FRONT PANEL

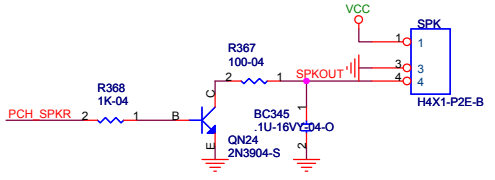
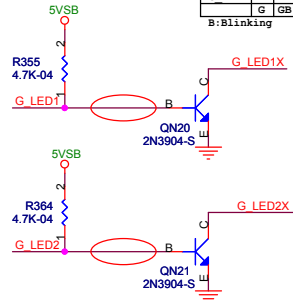


F PANEL



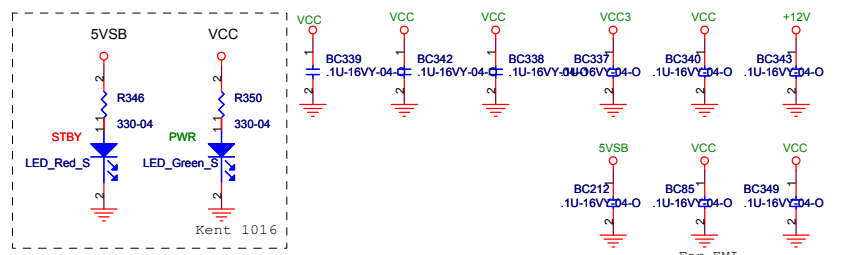
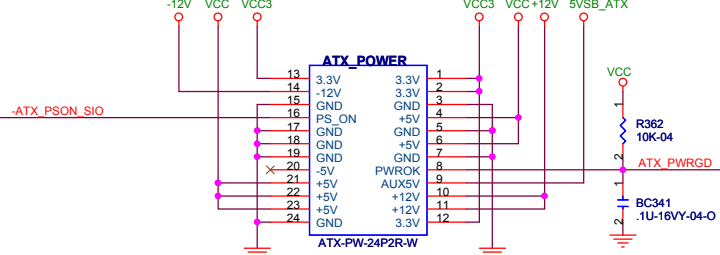
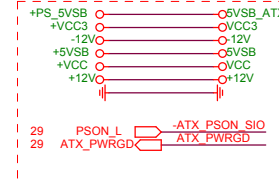
S0	S1	S3	S4	S5
G LED1	L	B	B	L
G LED2	H	H	L	L
G	GB	YB	OFF	OFF

B: Blinking



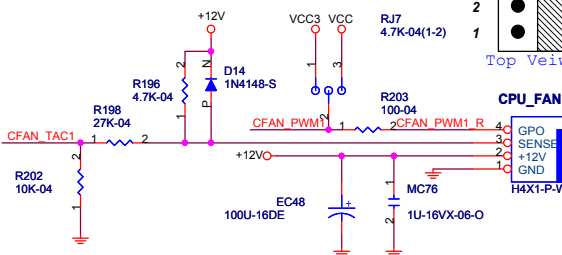
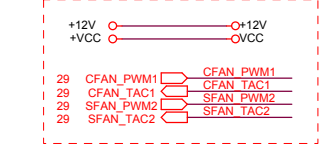
POWER CONNECTOR

External Connection

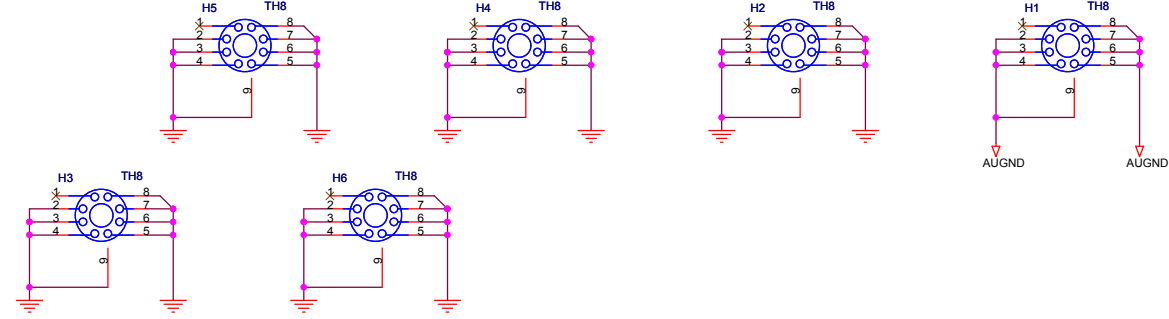
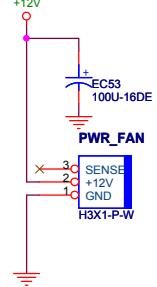
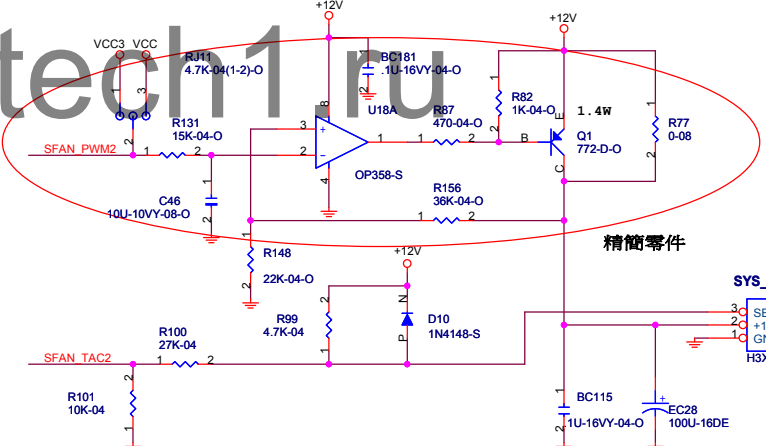


FAN

External Connection



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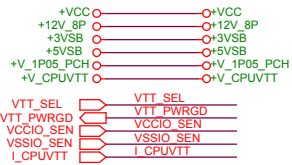


Title: Front Panel,FAN,PowerConn

Size Custom: Document Number: P67H2-A3

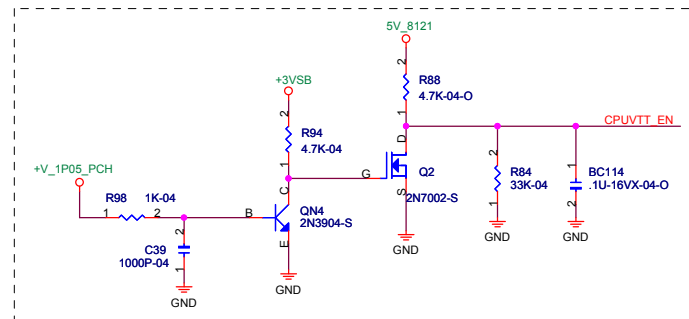
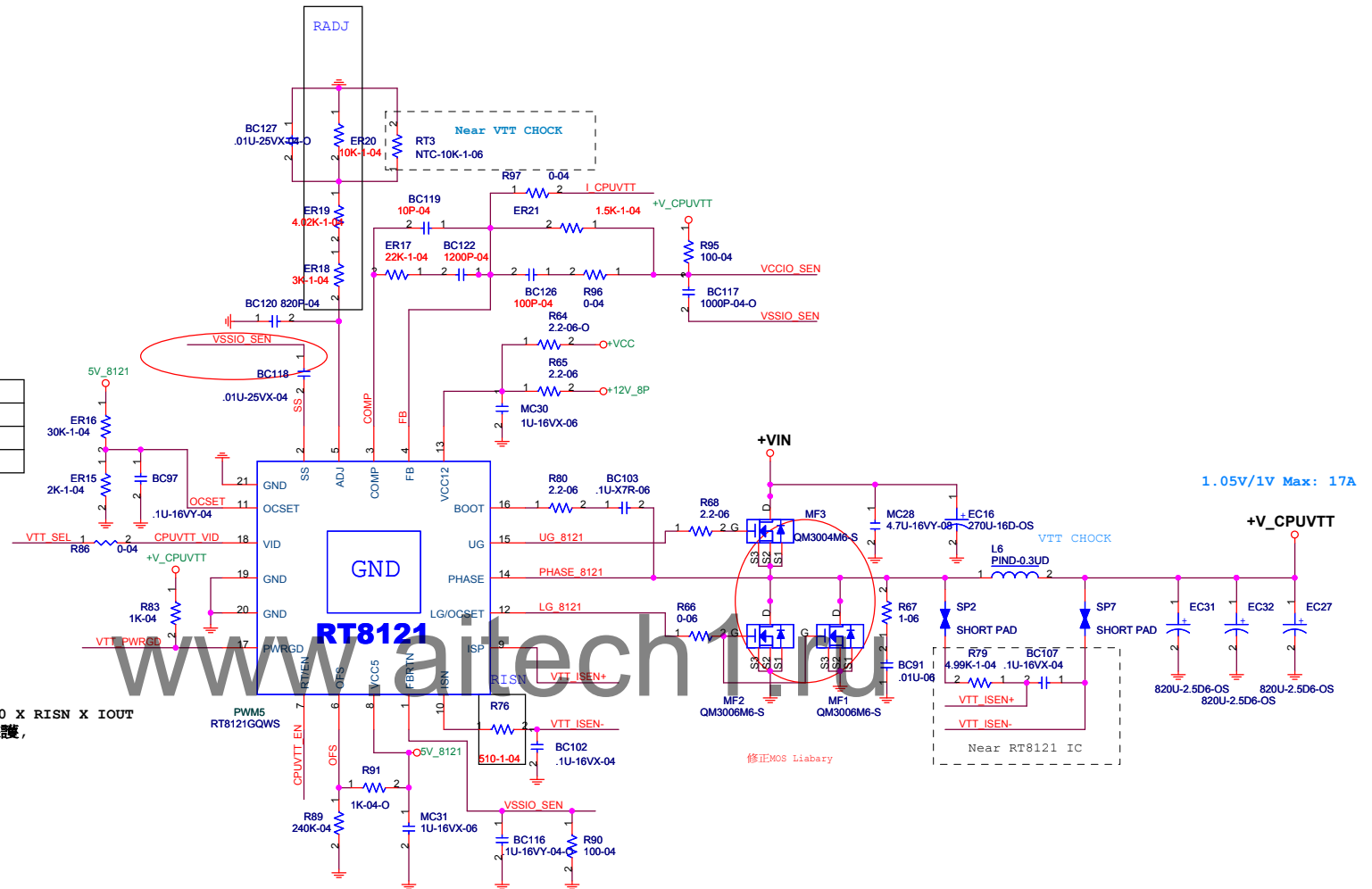
Date: Sunday, September 19, 2010 Sheet 31 of 37

## External Connection

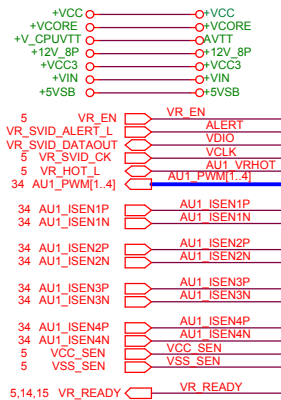


VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

$V_{ADJ} = LL \times I_{OUT} = DCR \times RADJ / 20 \times R_{ISN} \times I_{OUT}$   
 OCP設定方式就是VADJ > VOCSET 時保護，



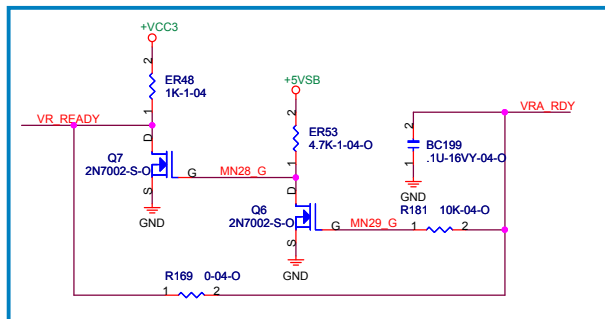
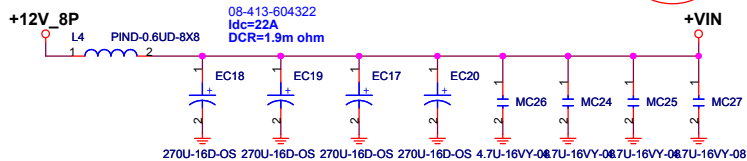
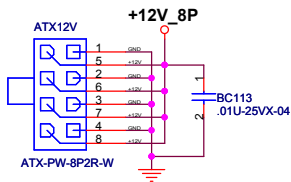
## External Connection



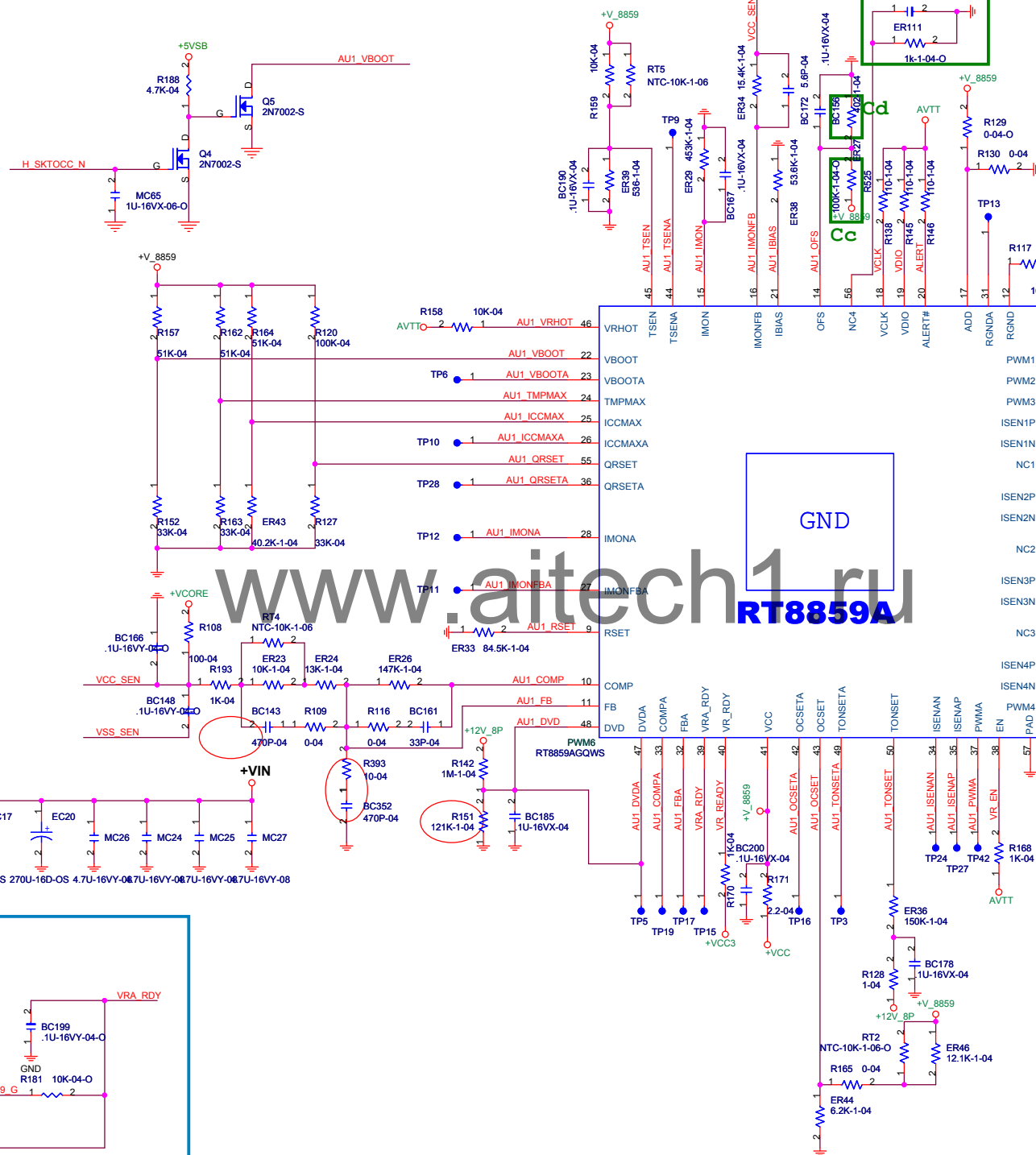
DEL VAXG

11 I\_VCORE → I\_VCORE

5,29 H\_SKT0CC\_L → H\_SKT0CC\_N



For VR\_READY Power On Sequence

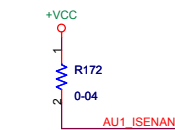
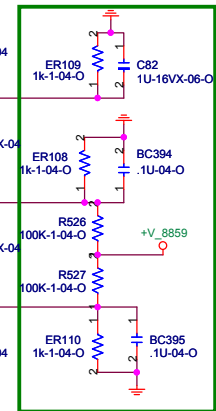


## BOM Difference

	RT8859A	RT8859M
Ca	X	V
Cb	X	V
Cc	X	V
Cd	402-1-04	1k-1-04

AU1\_OFS 2 5112 1 I\_VCORE 0-04

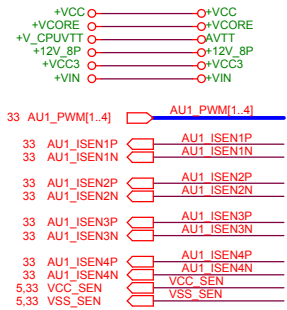
Cb



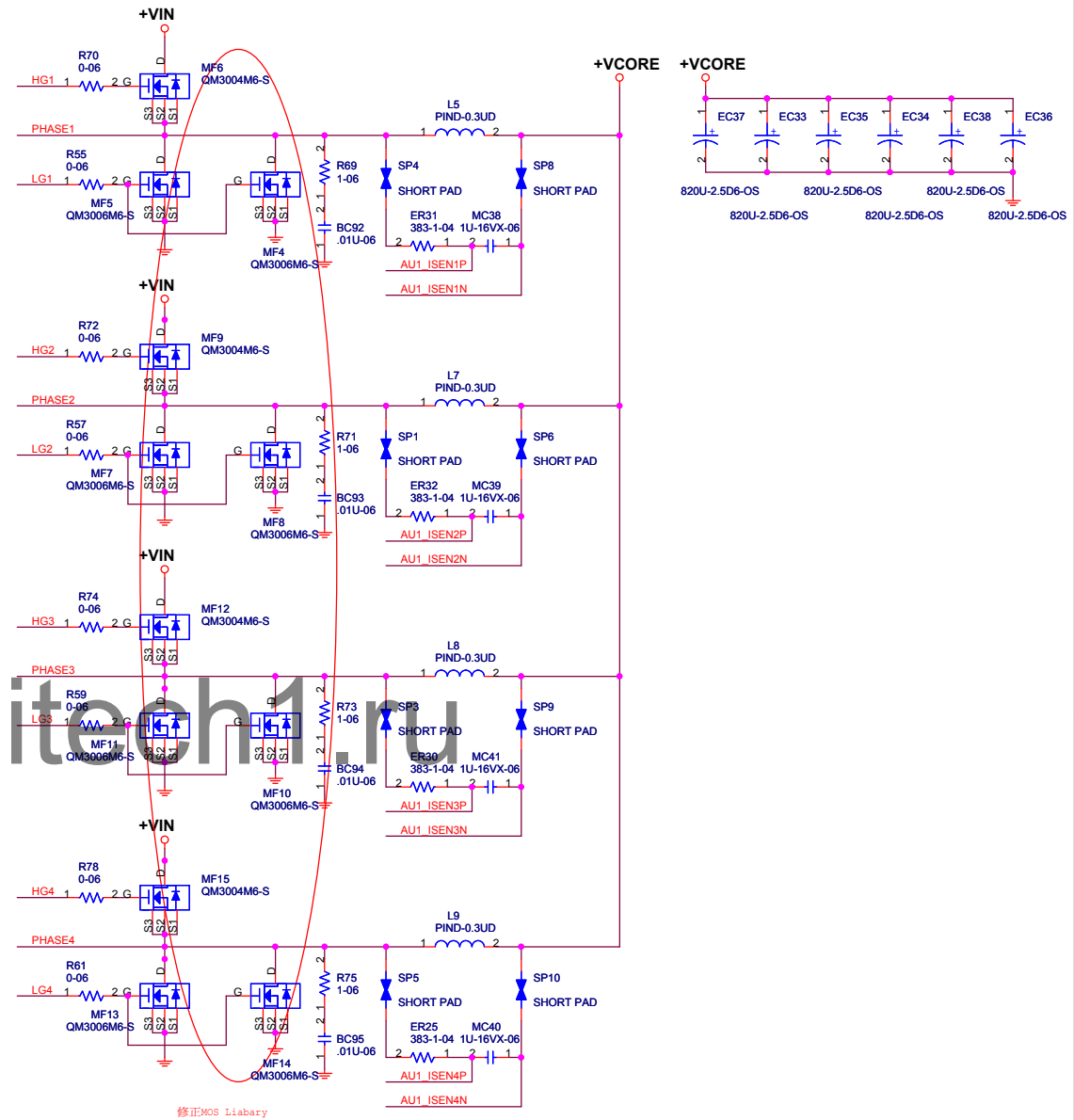
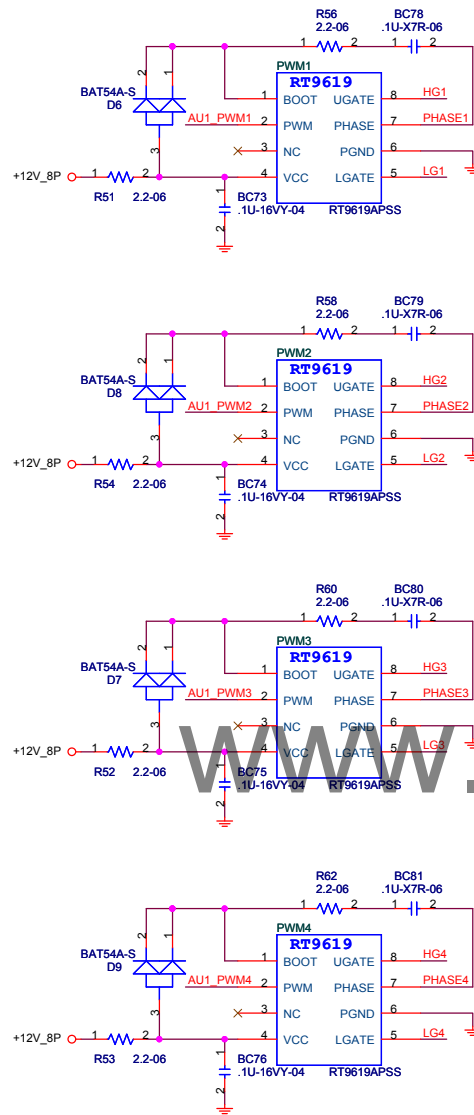
Elitegroup Computer Systems

Title	DC/DC VCORE/VAXG RT8859A		
Size	Document Number	P67H2-A3	Rev 1.0
Custom			
Date:	Thursday, September 16, 2010	Sheet	33 of 37

## External Connection



DEL VAXG



修正MOS Libary

DEL VAXG

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching RT8859 4+1 phases
Vcore:0.65~1.3V
Vaxg:0.65~1.3V

Switching RT8121 1 phase
V_CPU_VTT:1.05V

Linear LM324
VCC_SA:0.925V (0.85V)

Switching RT8105
V_DIMM:1.5V

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S0

LDO APL5336
DDR_VTT:0.75V

Linear LM324
PCH_CORE:1.05V

Intel Sandy Bridge CPU		
VCCP	VTD	85A, ICCMAX 112A
VAXG	NA	NA
VCCIO	1.05V(1V)	17A(I <sub>max</sub> )
VCC_SA	0.925V(0.85V)	8.8A(I <sub>max</sub> )
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Intel Cougar Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLLA	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.159A
Vcc3_3	3.3V	0.409A
VccADAP	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.097A
VccSUSHDA	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

Battery 3V
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LAN Realtek RTL8111E		
VDD3P3	3.3V	90mA
VDD1P0	1V	332mA
CTRL1P0 internal LVR Output		

SUPER I/O IT8721		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC892		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

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Switching RT8015A
V_ME:1.05V

Linear LM324
V_SFR:1.8V

5VDUAL Switch IC UP7536
USB_5V

X16 PCIe Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

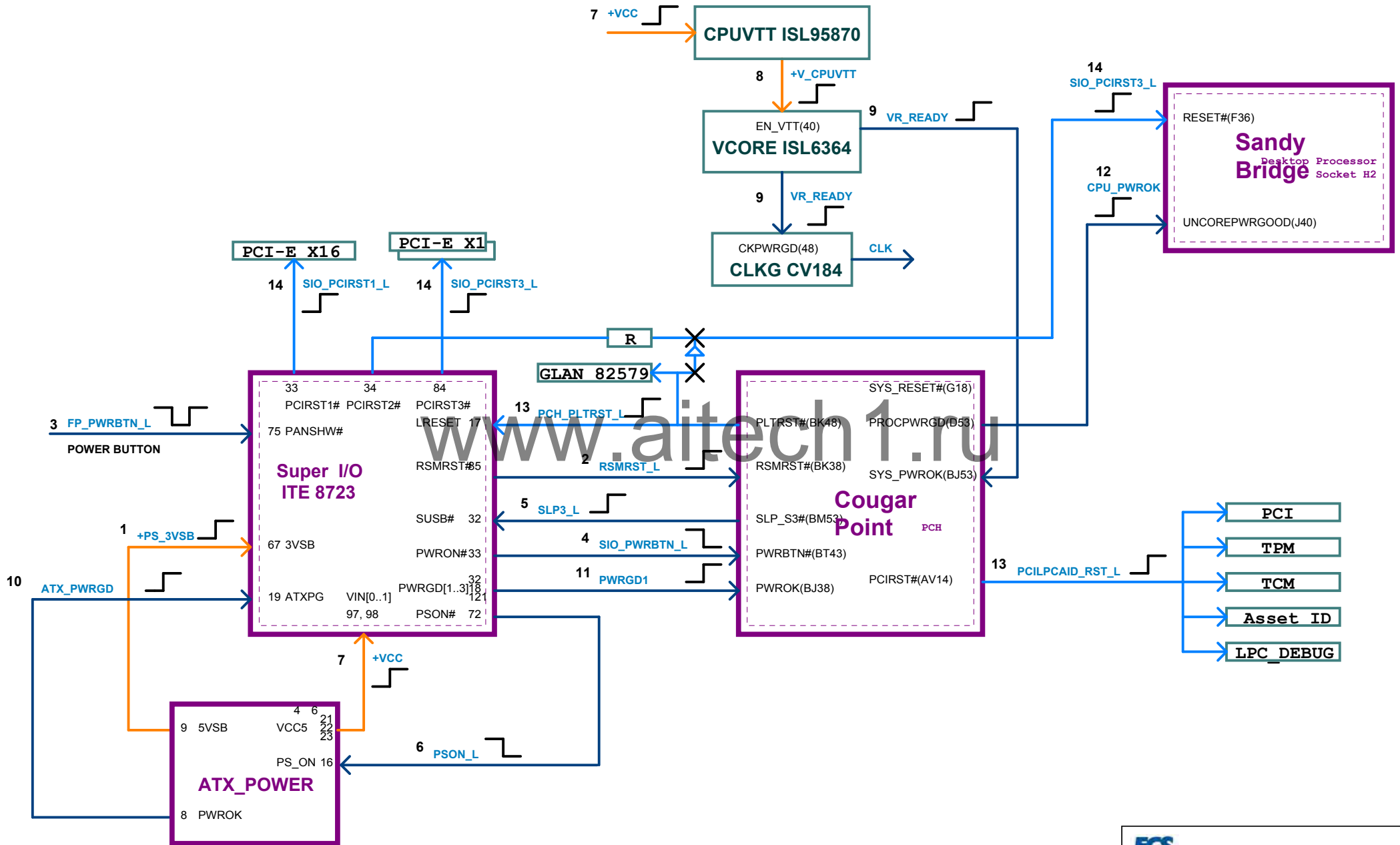
X1 PCIe Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)

USB X4 Header	
VDD	5VDual
2.0A	2.0A

USB X4 IO	
VDD	5VDual
2.0A	2.0A

PS/2	
5VDual	1.0A





**NOTE:**

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

